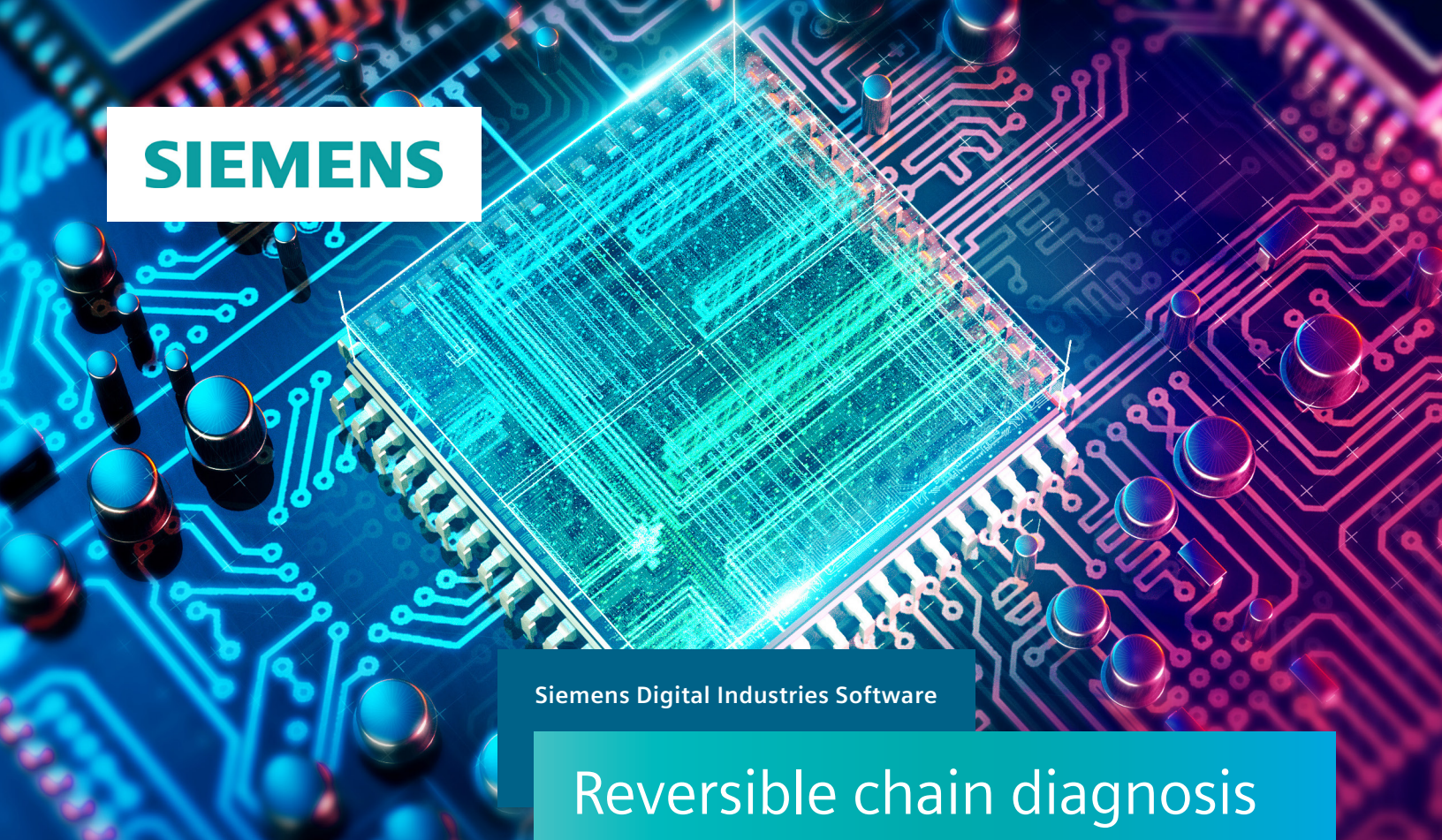


The background of the top half of the page is a close-up, artistic photograph of a circuit board. It features various electronic components like capacitors and integrated circuits, with glowing blue and purple light trails and patterns overlaid, suggesting digital data flow or diagnostic processes. The Siemens logo is prominently displayed in the upper left corner.

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Reversible chain diagnosis

Improve scan chain diagnosis resolution by 4X

Executive summary

For advanced technologies, the industry is seeing very complicated silicon defect types and defect distribution. One consequence is that scan chain diagnosis becomes more difficult. To improve the resolution of scan chain diagnosis, Tessent Diagnosis can use new scan chain test patterns to leverage a reversible scan chain architecture.

This paper describes the novel scan chain architecture that enables bi-directional shift operations during chain diagnosis and delves into the pattern generation needed to create a pattern set that allows diagnosis down to single cells. This new technology comprising scan chain design and diagnosis improves chain diagnosis resolution by 4X.

Jayant D'Souza, Siemens Digital Industries Software

Introduction to scan chain diagnosis

Scan chains help you test complex chip designs. But how do you test the scan chains themselves when they go wrong? Scan chain diagnosis has been leveraged to identify yield limiters in all phases of yield ramp.

For new technology nodes, test chips are used as characterization vehicles during the technology qualification stage. This stage is typically characterized by low yield and the volume of test chips is typically low. Scan chain failures could account for up to 66% of the chip failures (the rest being logic defects) [1]. Since full scan diagnosis is limited by the small volume, chain diagnosis along with electrical fault isolation (EFI) techniques are relied upon to isolate defects in the test chip for yield learning.

Following a successful technology qualification phase is the product qualification phase where the test chips are more representative of the design. In this phase, while the volume of chips is low, the proportion of chain failure rate to logic failure rate is roughly the same [2].

During this product qualification phase, the goal is to identify any product-specific and systematic issues to achieve entitlement yield. Entitlement yield presents

the best possibility of profitability for a semiconductor company. Economic reasons, therefore, dictate that this goal be achieved in as short a time as possible.

With new, advanced technology nodes (such as 5 nm and below), economic pressures for higher and quicker profitability have intensified. With the ongoing semiconductor shortages (from 2021), semiconductor demand far outweighs the supply and has added to the economic pressures of achieving this entitlement yield as quickly as possible [3].

In each of these phases, scan chain diagnosis and electrical fault isolation (EFI) play critical roles in successfully achieving the goals of yield ramp. When silicon defects affect the scan chain path, chain diagnosis and EFI are employed to pinpoint the location of the defect and determine a root cause. Tessent can now leverage reversible scan chain architectures (Figure 1) to generate patterns that improve scan chain diagnosis resolution.

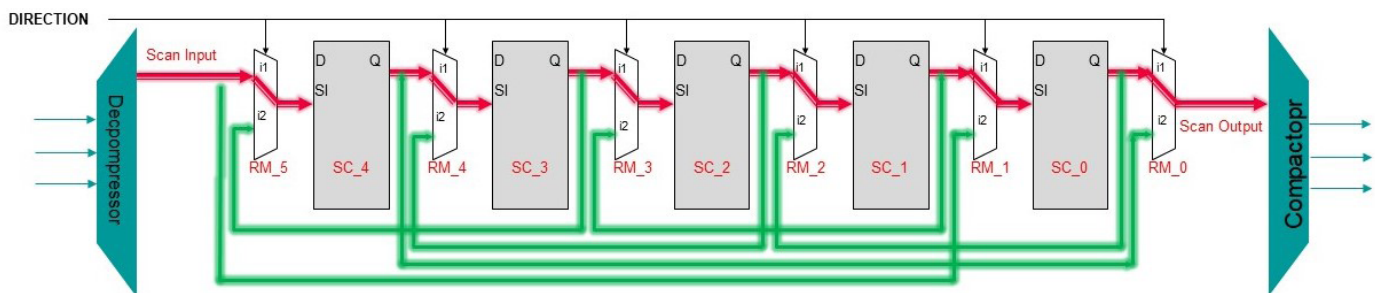


Figure 1. Tessent leverages the existing reversible scan chain architecture to generate patterns for diagnosis.

Scan chain diagnosis

Scan chains enable scan testing of digital ICs. Scan patterns generated for the design comprise chain and scan tests. Chain tests validate the integrity of the scan chains before testing the logic in an IC. Scan tests, leverage the scan chains in the design to place the design in a functional state and then capture the response of the design in that functional state.

Typically chain diagnosis requires both failing chain test patterns and failing scan patterns. The diagnosis process is a two-step process – first, the failing chain(s) is determined. Chain diagnosis is illustrated in figure 2.

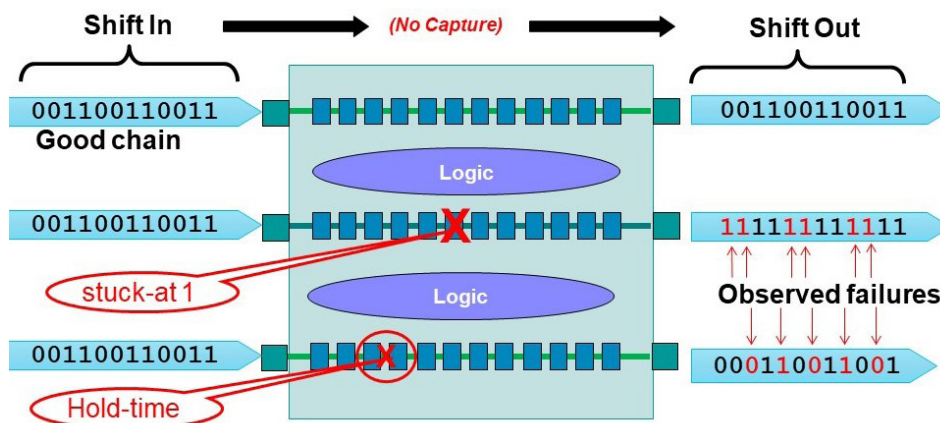


Figure 2. Identifying failing chains and defect type.

In this step, only the chain tests are required. Since chain tests simply shift data through the scan chains. The expectation is that the data shifted in is also shifted out without change. Any differences in the observed chain values as data is shifted out are deemed failures. The differences between the expected and measured scan chain responses produce a signature that is used to determine the failing chain and defect in the failing chain(s).

At the end of this first stage, only the failing scan chain(s) and the defect type are identified. The location of the defect could be anywhere in the entire range of scan cells in the defective scan chain.

Next, the failing scan patterns are used to determine the possible suspect scan cells in the failing chain that could contain the defect, as shown in figure 3.

The assumption is that the defect(s) on the failing chain can affect the values in the scan cells on the good chains. Therefore, by examining the failing cycles on the good chains, a likely set of defective scan cells can be produced.

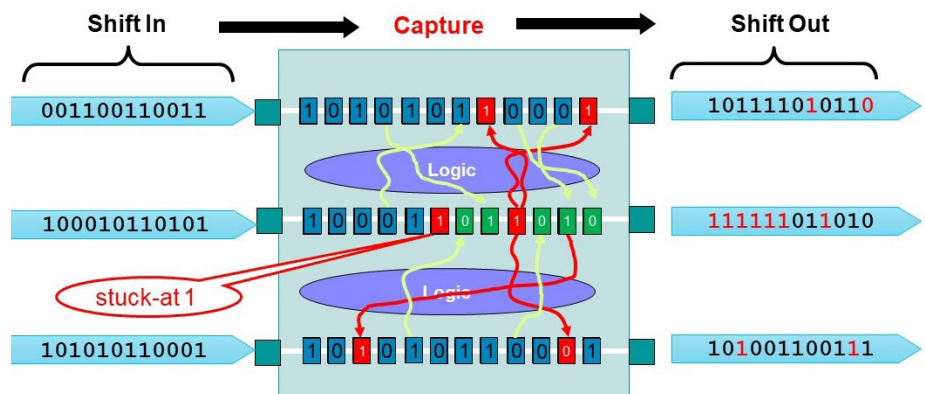


Figure 3. Identify suspect scan cell(s) for a defect.

Reversible chain technology

As seen in figures 2 and 3, scan chains typically allow the shifting of data in a single direction. With the new reversible chain technology, the scan chains are designed so that they can shift in the reverse direction as well. Figure 4 illustrates the construction of the scan chains so that bi-directional shifting can be achieved.

DIR

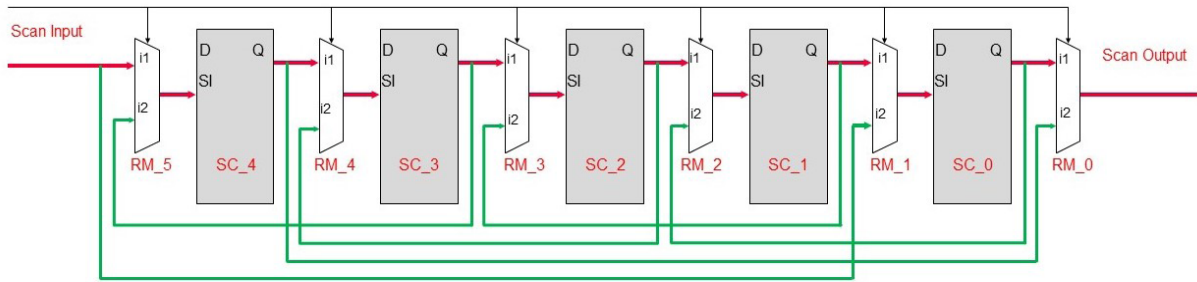


Figure 4. Scan chains for bi-directional shifting.

The scan chains are stitched so that paths exist that will allow the shifting of scan data in both directions through the scan chains. The direction in which data is shifted in the scan chains is controlled by a direction control pin (DIR) as illustrated above. When scan chains are created in this manner, direction of data shifted through the scan chains is controlled by the DIR pin.

Left to right (L2R) shift operation

When the directional control pin DIR is set to 1, data is shifted through the scan chains from left to right as highlighted by the path in red. This can be referred to as the default shift operation, shown in figure 5.

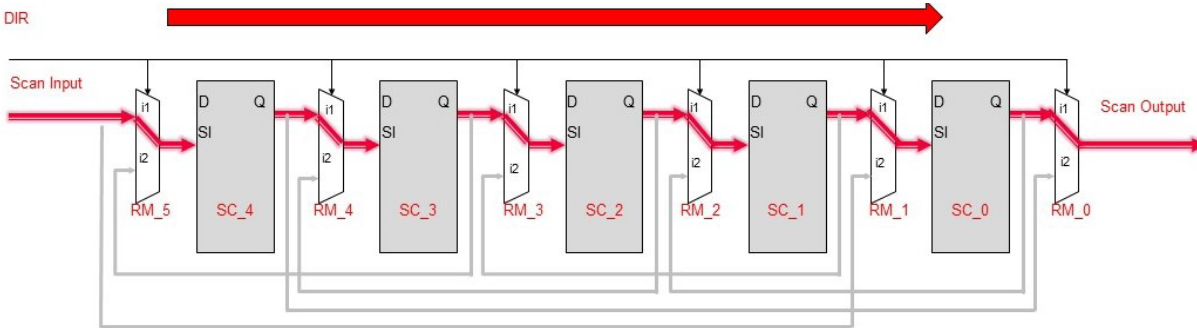


Figure 5. L2R shift operation.

Right to left (R2L) shift operation

When the directional control pin DIR is set to 0, data is shifted through the scan chains from right to left as highlighted by the path in green. This can also be referred to as the reversed shift path, shown in figure 6.

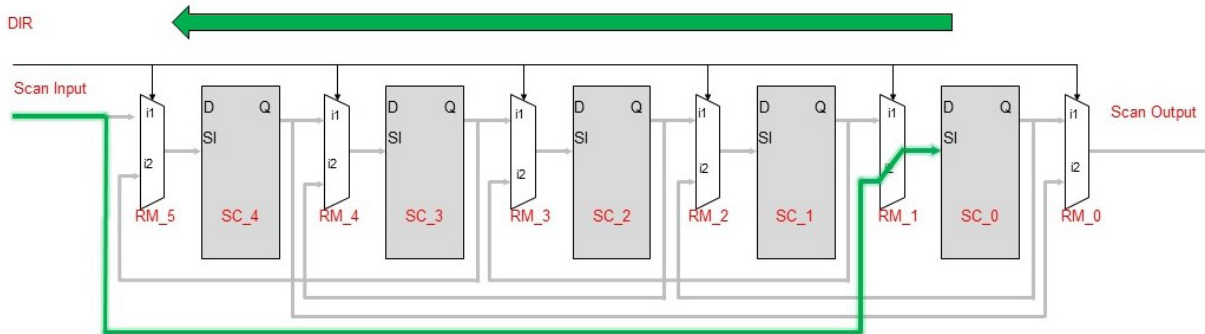


Figure 6. R2L shift operation.

Reversible chain diagnosis

When reversible chain hardware is inserted into the design as described in the previous section, chain test patterns can be generated for each of the directions of data shift in the scan chains.

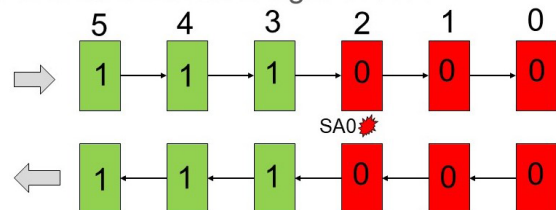
The chain test patterns are generated so that the data is loaded from L2R and unloaded from R2L directions as described above. Additionally, patterns are also generated so that data is loaded from R2L and unloaded from L2R as well.

This bidirectionality of the scan chains and the patterns is leveraged by chain diagnosis. To illustrate how the diagnosis process works, let's assume that a single permanent defect exists on cell 2 of a scan chain that behaves like a stuck-at 0 fault (SA0). The diagnosis occurs in 4 steps as follows:

In steps 1 and 2, we load the data 111111 from left to right (L2R) and unload this data from right to left (R2L). shown in figure 7. Due to the defect at cell 2, the unloaded data is 111000.

In the next steps step 3 and 4, the same pattern data is loaded from right to left (R2L) and unloaded from left to right (L2R). So the pattern data 111111 is loaded from L2R and unloaded from R2L as illustrated in figure 8. Due to the defect at cell 2, the unloaded data is 110000 after Step 4.

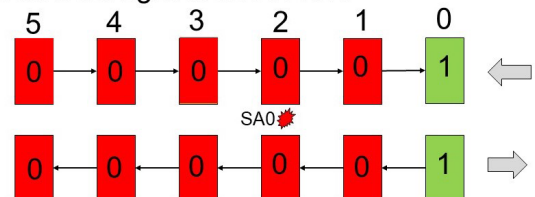
Step 1: load from left to right 111111



Step 2: unload from right to left 111000
Diagnose the **leftmost** defect location

Figure 7. Steps 1 and 2 of reversible scan chain diagnosis.

Step 3: Load from right to left 111111



Step 4: unload from left to right 000001
Diagnose the **rightmost** defect location

Figure 8. Steps 3 and 4 of reversible scan chain diagnosis.

The unloaded data from the scan chains from Step 2 and Step 4 is shown in figure 9. The cell position 2 shows the same difference in both directions indicating the defect location.

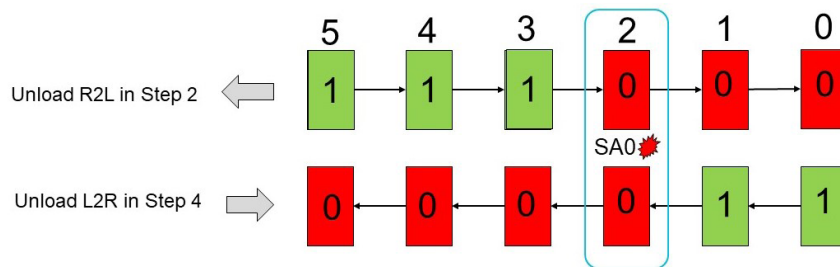


Figure 9. Unloaded data from the scan chains from Step 2 and Step 4.

Design flow

The advantage of this method is that only chain test patterns are required for diagnosis. Since only failing chain test patterns are required, the diagnosis process also runs much faster. Enabling reversible chain diagnosis requires small changes to the design and the design flow. Reversible chains are predicated on the reversible scan paths of the scan chains in the design. The implication is that there is an impact on the design hardware – i.e. the scan chains have to be stitched in a manner that accomplishes shifting in either direction. Stitching of the reversible chains into the design can be done in a variety of different ways. One such method is described below that leaves the regular design flow untouched. Figure 10 illustrates.

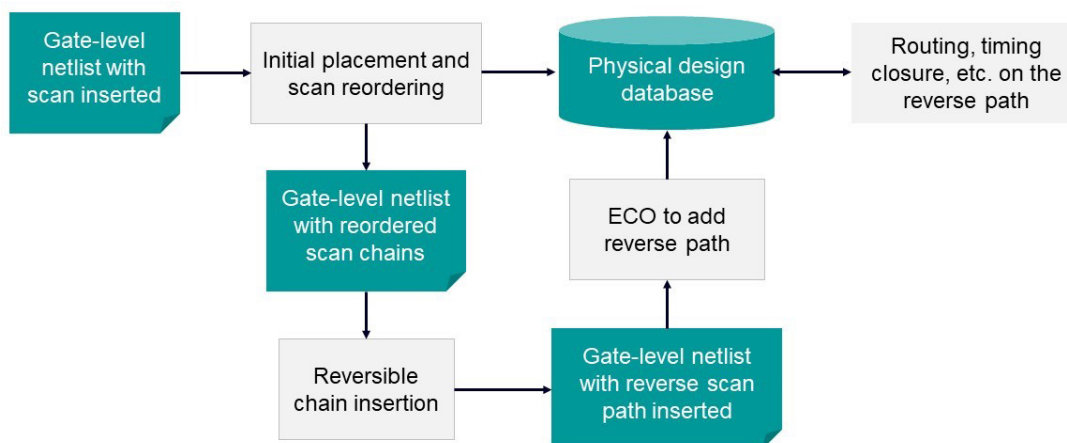
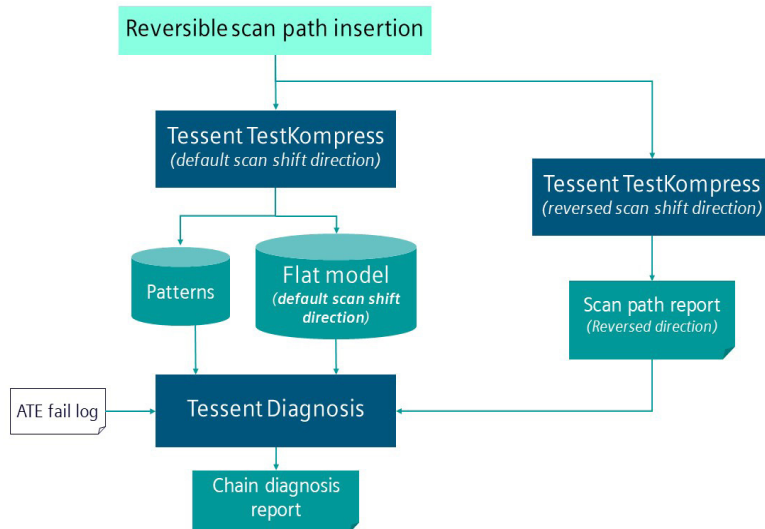


Figure 10. Design flow for reversible scan chain diagnosis.

In this ECO-based flow, the reversible scan path is added to the final netlist using ECO scripts in the place and route (PNR) tool. It is important to note here that this ECO is applied after the netlist has been hardened and scan chain ordering is complete thereby leaving the design flow untouched. Scan chain ordering cannot be revised once the reversible scan paths have been added.



The next part of the design flow is pattern generation and diagnosis. During this stage, chain patterns are generated by the ATPG tool automatically for both directions, as shown in figure 11. Additionally, a scan path report must be generated for reversed direction by tracing the scan chains in the reversed direction. This report must be supplied during diagnosis. Once an ATE fail log is available, the flat model, patterns and ATE log are consumed by Tessent Diagnosis along with the scan path report of the reversed direction to produce a chain diagnosis result.

Figure 11. Pattern generation and diagnosis in reversible scan chain diagnosis.

Silicon results of reversible chain diagnosis

Reversible chain technology has a large positive impact on chain diagnosis. A silicon experiment was conducted in a volume diagnosis setting using a test chip on a leading-edge technology node. The results of that experiment were confirmed by failure analysis. Reversible chain diagnosis performance was evaluated and table 1 shows the improvements that were seen.

Evaluation Measure	Improvement
Defective device detection	1.5X increase
Diagnosis runtime	4X reduction
# of single suspect cases (Resolution)	6X increase
# of suspects in defective chains (Resolution)	3.9X reduction
Physical area reduction	
Enclosing circle	2X
Enclosing rectangle	2.4X
Net area	1.8X
Cell area	7X

Table 1. Measured improvements with reversible scan chain.

Implementing reversible chains also carries a design impact. Table 2 shows the key metrics observed for design overhead.

Key Performance Indicators	Change
Leakage Power	11% increase
Cell count increase	11% increase
Routing wire length increase	15% increase
Final PRO Utilization	~5% increase

Table 2. Design impacts of reversible scan chain.

A tangible benefit was seen when using the reversible chain diagnosis technology in the design. The design overhead to achieve almost ~4x better resolution with a 4x improvement in run time comes at a small cost to area overhead as shown above.

Conclusion

Reversible chain diagnosis technology is proven to improve chain diagnosis resolution by 4X with an improved diagnosis run time of 4X. Using this technology can certainly aid in the race to entitlement yield, especially at leading technology nodes.

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2. "Survey of Scan Chain Diagnosis"- Huang, et al (IEEE Design & Test of Computers – vol 25, Issue 3, May – June 2008)
3. "A Technique for Fault Diagnosis of Defects in Scan Chains" – Guo, et al (ITC 2001)

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