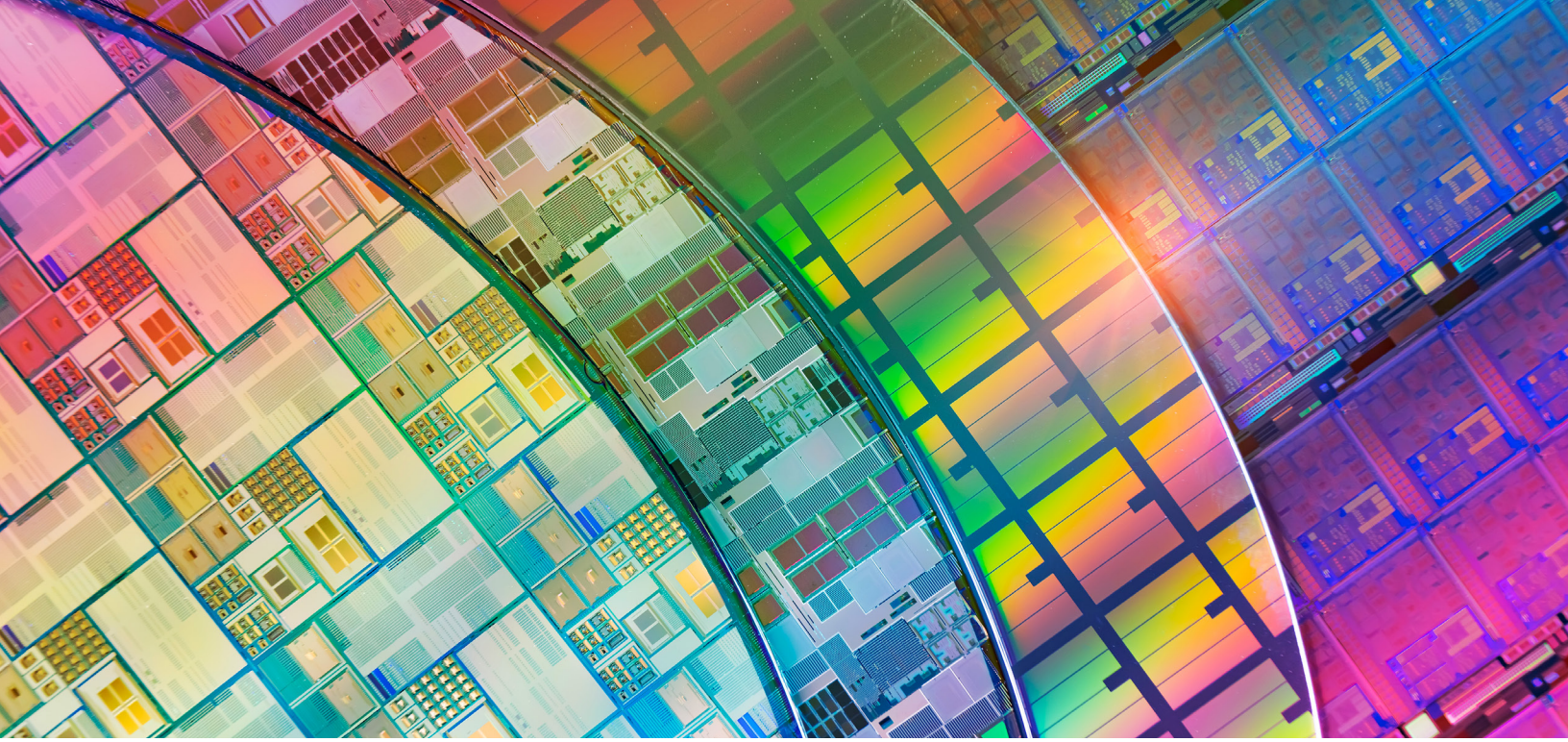


DIGITAL INDUSTRIES SOFTWARE

Avery Verification IP for AMBA

Your solution for AMBA® compliance validation

Benefits

- Delivers a comprehensive, advanced UVM verification solution
- Boosts verification efficiency
- Enables development of more complex tests
- Supports more complex topologies, such as multi-path and multi-link solutions
- Increases effectiveness with core-through-chip-level tests

Summary

AMBA® ACE and CHI coherent interconnect technologies enable an entirely new class of high-performance datacenter applications in areas of machine learning, network processing, storage off-load, in-memory database, and 4G/5G wireless technology. Processor architectures and accelerators can now seamlessly operate over cache coherent interconnects using the right combination of general-purpose processors and heterogeneous acceleration devices, such as FPGAs, GPUs, network/storage adapters, intelligent networks, and custom ASICs.

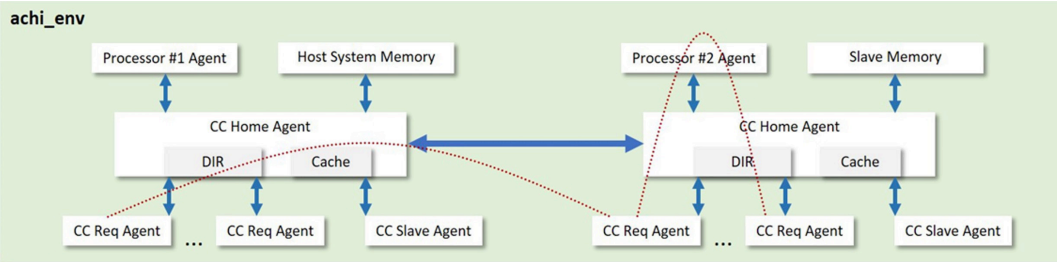
Avery AMBA VIP provides a comprehensive verification solution featuring an advanced UVM environment that incorporates constrained random traffic generation; robust packet, link, physical layer controls, and error injection; protocol checks, coverage, and functional coverage; protocol analyzer-like features for debugging; and performance analysis metrics. With the advanced capabilities of Avery VIP, you can work more efficiently, develop more complex tests, and work on more complex topologies, such as multi-path, multi-link solutions. Avery compliance test suites offer effective core-through-chip-level tests, including those used in compliance workshops as well as extended tests developed by Avery to cover specification features.

Highlights

- APB, AHB/AHB5, AXI3/AXI4/AXI4-Lite/AXI5, ACE/ACE5, CHI.Ea, CXS.B
- Master, slave, and interconnect models in active and passive mode monitors
- All models support random wait states on address, data, and response channels, including programmable response behavior using request matching
- User-defined slave read/write response queues
- Full data interleaving and multiple outstanding requests and out of order responses
- Plug and play ARM SystemVerilog assertions
- Supports ARM FastModels, allowing hybrid simulation of CPU subsystems for an overall HW/SW SoC verification process
- Includes CHI and ACE cache coherency test suites and a comprehensive set of examples
- Native SystemVerilog and UVM implementation
- ACE/CHI models N-way or fully associative cache, automatic cache management operations, and replacement strategies, including user-defined, RR, FIFO, LRU, random with backdoor, and silent automatic state transitions
- Complementary CCIX VIP also available

AMBA 5 CHI VIP

- CHI home agent interconnect with directory, request, and slave agents
- Passive monitor performs snoop response verification
- Cache state trackers and transaction-level protocol trackers improve debug
- Supports CXS.B interface for CXL/CCIX-CHI bridging, enabling unit-level verification by bypassing PCIe layers
- Cache coherency verification test suite for CXL/CCIX and CHI systems
- Protocol checking
- Performance measures
- Functional coverage



End-to-end CHI environment.

```
==> @190 achi_HN0_MP1 receive TXREQ FLIT from Master
  Opcode: WriteUniqueFull    SrcID: 1                TgtID: 0      TxnID: 6e Address: 'h90000dbc
      NS: NonsecureAccess     Size: 6                  QoS: e       LPID: 1   MemAttr: d
LikeShrd: 1                  Order: NoOrdering    Exclusive: 0 AllowRetry: 1
PCrdType: 0                SnpAttr: InnerSnoop   ExpCompAck: 1

               <== @270 achi_HN0_MP1 send out a response transaction from queue:
                 Opcode: DBIDResp   SrcID: 0         TgtID: 1         TxnID: 6e        CCID: 0
                RespErr: OK          Resp: I           QoS: e          DBID: cf

==> @410 achi_HN0_MP1 receive TXDAT flit from Master
  Opcode: NCBackWrData          SrcID: 1                    TgtID: 0         TxnID: cf        CCID: 3
 RespErr: OK                     Resp: I                     QoS:             DBID: f3      DataID: 0
    Data: 72, b4, dd, 0d, 4b, 79, 9e, fd, 7b, 8f, 03, e3, 1d, b1, 44, 95,
          e0, ed, 52, f8, 8d, 52, 84, 46, 8c, 90, 17, 6a, 84, aa, 7c, 60,
          ba, 8b, a6, 25, 32, a2, 49, 14, 3d, 4b, 5c, 47, 86, 39, b4, d0,
          2c, 8c, 07, 6a, 11, e8, 4b, 73, ec, 23, a4, c9, 39, df, d4, 67

               <== @490 achi_HN0_MP1 send out a response transaction from queue:
                 Opcode: Comp       SrcID: 0         TgtID: 1         TxnID: 6e        CCID: 0
                RespErr: OK          Resp: I           QoS: e          DBID: cf
```

Home node monitor shows CHI messages across all ports.

```
      Action Addr.  Line Addr.    State      Cnt    Data                                 Action
      ============  ============  =========  =====  ===================================  ====================
 480  92000b69      92000b40       I ->  I   00     -- -- -- -- -- -- -- -- (  7:  0)  trans (WRNoSnoop)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 15:  8)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 23: 16)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 31: 24)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 39: 32)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 47: 40)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 55: 48)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 63: 56)
 920  92000b69      92000b40       I ->  I   00     -- -- -- -- -- -- -- -- (  7:  0)  trans (WRNoSnoop)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 15:  8)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 23: 16)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 31: 24)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 39: 32)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 47: 40)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 55: 48)
      ------------  ------------  ---------  -----  -- -- -- -- -- -- -- --            ( 63: 56)
```

AMBA ACHI BFM cache monitor “achi_HN4_RN19_cache_tracker.txt”.

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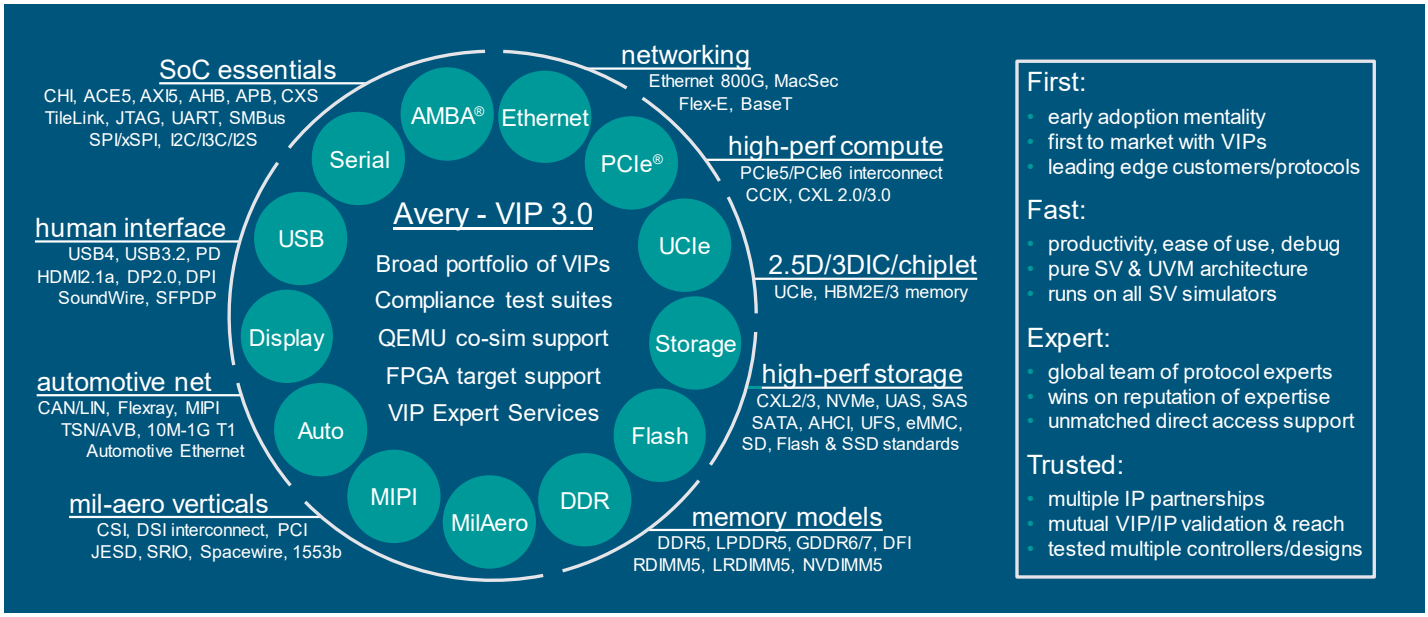

Avery Verification IP portfolio (Feb 2024).

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