

SIEMENS
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Questa Sequential Logic Equivalence Checking (SLEC) app

Automated and exhaustive formal analysis

Benefits

- Automated hierarchy, instance, and signal name-mapping
- Quick root-cause debug guides users directly to source of an issue
- No knowledge of formal or assertion languages is required
- No testbench needed, enabling verification to start early in the design phase, before a simulation testbench is ready
- Powerful Tcl API for custom reports and flows

Features

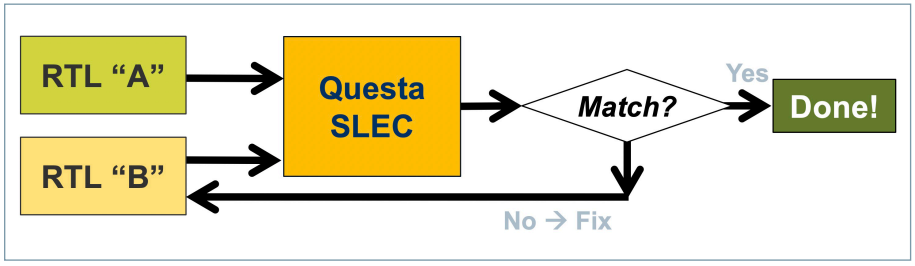
- Runs deep formal analysis on automatically mapped and correlated RTL designs to compare their behaviors for all inputs and all time
- Exhaustive approach means the analysis traverses the entire state space, revealing unexpected corner-cases that can be missed by other verification methods
- Checks all sequential behaviors, enabling comparison of IPs with unrelated state encodings

Quite a few high-value verification tasks involve the comparison of a circuit to a close equivalent that's been modified in a small, yet operationally critical way. For example, sometimes new logic is required to reduce dynamic power consumption, an ECO is needed at the last minute, or the impact of stuck-at or transient faults must be evaluated. While each of these tasks can be addressed with RTL simulation, doing so can take weeks — even months — of testbench development and simulation debug. Even worse, the results from even the most well-designed constrained-random simulation environment will not be exhaustive, leaving the door open for functional bugs that were unintentionally created by the added logic.

The asynchronous reset domain crossings (RDC) that arise create metastability and signal reconvergence issues in the reset signaling networks — similar to the failures seen in asynchronous clock domain crossings (CDC). Just as with CDC phenomena, the metastability induced by these asynchronous RDCs cannot be modeled or exhaustively covered by digital simulation, leaving designers open to the considerable risk of unpredictable chip behavior when samples come back from the fab, or worse, in the field.

Automated sequential logic equivalence checking

A sequential logical equivalence check (SLEC) formally verifies that two sequentially different designs are functionally equivalent. The Questa® SLEC app performs an exhaustive, formal-based analysis of two RTL designs in only a few hours — even minutes — depending on the design sizes and parameters. This frees the user from having to manually create and maintain testbenches and re-run massive, time and resource intensive simulation regression suites.



The Questa SLEC app uses formal analysis to exhaustively compare two blocks of RTL code, identifying any differences in the output behavior of the two designs for all inputs, and for all time.

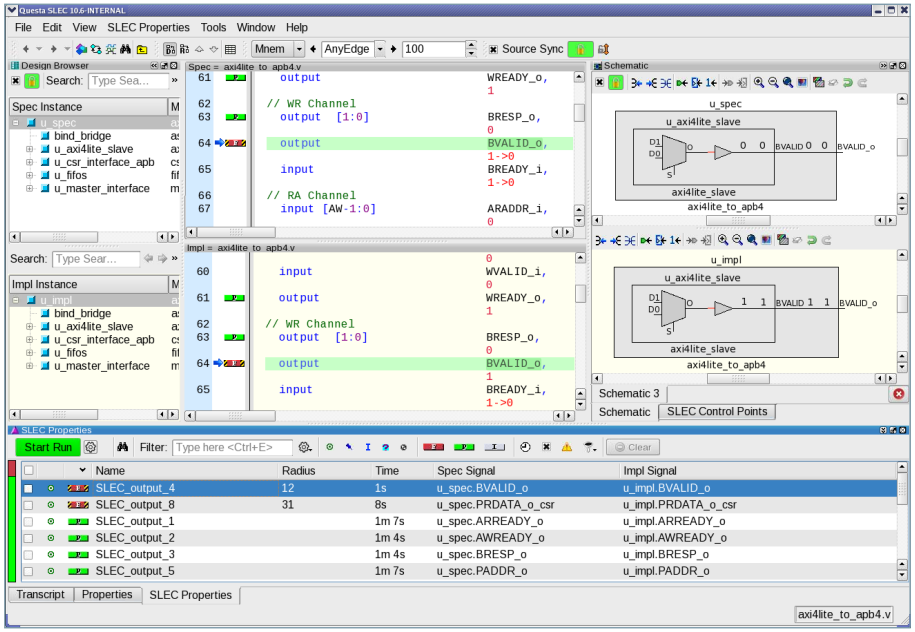
Questa SLEC

In particular, the following verification use cases dramatically benefit from a Questa SLEC analysis:

- Design optimization (state machine optimization, pipeline reordering, etc.)
- ISO26262-related fault/single event upset (SEU) safety mechanism verification
- Bug fix and ECO verification: avoiding time consuming re-simulation after making minor changes
- Low power clock gating logic insertion

All discrepancies are summarized in concise reports so users can quickly determine the severity of any issues that are identified.

Note: Pure logic equivalency checking (LEC) tools (like FormalPro) are for flows where the DUTs being compared have the exact same number of states — mainly for the purpose of verifying that the synthesis of RTL into gates was done correctly. In contrast, Questa SLEC is checking all sequential behaviors and, hence, can check that any modifications to the RTL do not affect the outputs.



Benefits and highlights

Ease of set up and use — Set up is expedited by enabling users to account for trivial mismatches of net or instance names as well as arbitrary levels of hierarchy, before the analysis is launched. No testbench or knowledge of formal or assertion languages is required. Automated incorporation of synthesis design constraints (SDC), Liberty models, and Unified Power Format (UPF) specifications further expedites bring-up.

Exhaustive results — The Questa SLEC app uses formal engines under-the-hood to exhaustively compare the "specification" and "implementation" RTL, identifying any differences in the output behavior of the two designs for all inputs and for all time.

Increased productivity — All discrepancies are summarized with concise reports in an interactive GUI so users can quickly determine the root cause and severity of any issues that are identified. Plus, via the standard Tcl API users can easily tailor input, run-time, and output reports to address specific verification tasks.

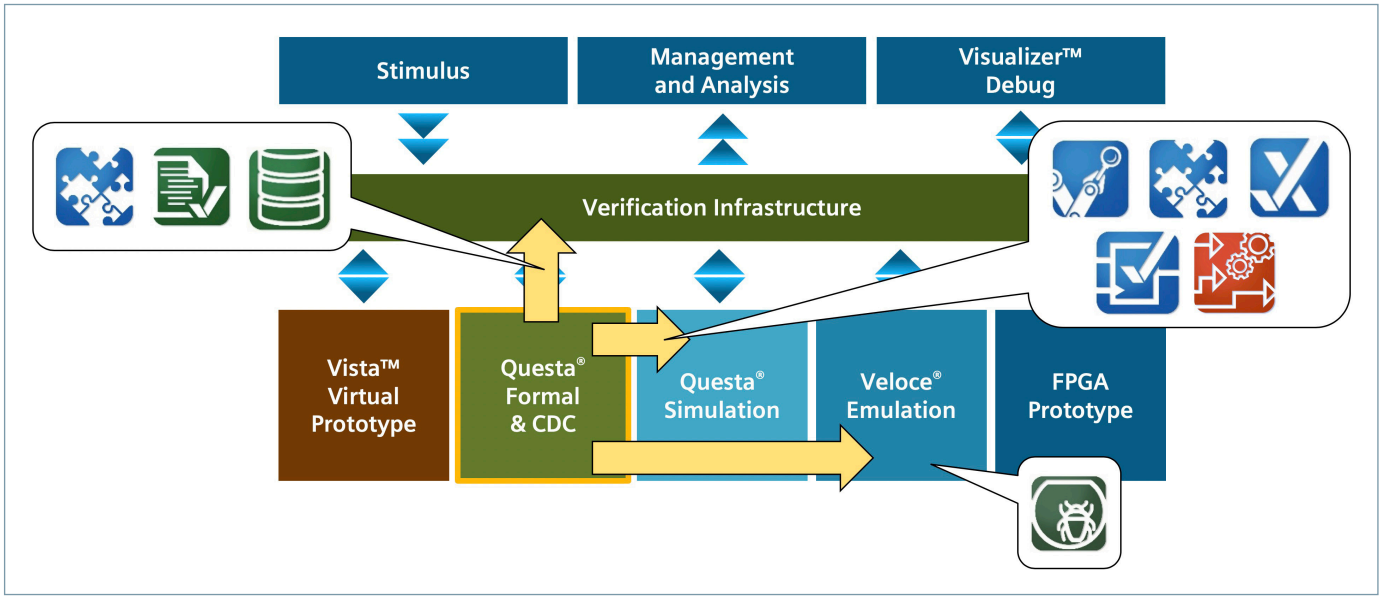
Familiar visualization — The Questa SLEC debug GUI leverages familiar schematics and waveforms where appropriate. Waveforms and generated schematics show precisely the output discrepancies between the two DUTs, along with the responsible control signals and data pathways.

High performance analysis — Dedicated, applied research and engineering investment in Questa SLEC analysis technologies have produced continuous improvements in wall clock performance, memory usage, and storage consumption. This means Questa SLEC regularly exceeds demanding scalability and resource expectations.

Enterprise Verification Platform

Built upon several powerful technologies and tightly integrated with Veloce® emulation, the Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources. The Questa Formal and CDC solutions are integrated with simulation and emulation, sharing common features such as verification management, compilers, debuggers, and language support for SystemVerilog, Verilog, VHDL, and more.

This enables users to select the best application or tool for the job and then combine results from all the engines to dynamically track the progress of the entire verification program.



The Enterprise Verification Platform

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