SIEMENS
Ingenuity for life

Questa Verification IP for flash memory

A comprehensive solution for exhaustive verification of flash controllers

Benefits

- Architected for ease-of-use and consistency across all protocols
- Comprehensive stimulus and standard-based test suites
- Exhaustive protocol checks
- UVM based testbench with ready-to-use components like monitors, loggers, and scoreboards
- Intuitive debug with transaction viewing and tracker files at various levels

Features

- Easy integration using memory modules
  - UVM and non-UVM testbenches
  - Single module for multiple part numbers
- Built-in analysis components
  - Protocol checkers
  - Transaction loggers
  - Functional coverage
- Configurable command and timers using file and backdoor APIs
- Memory operations (read/ write/ compare) using file and backdoor APIs

Supported Specifications

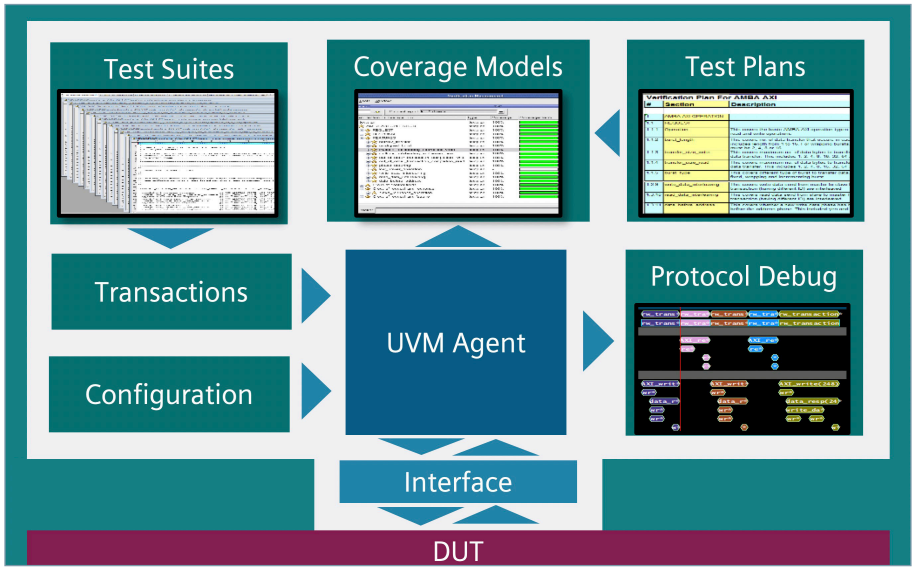
- ONFI Revision 4.1
- Toggle NAND
- SDCard Version 6.0
- SDIO Version 4.1
- eMMC Version 5.1
- Serial/Parallel NOR
- Micron, Winbond, Cypress, ISSI,
- Samsung part numbers
- Serial NAND

Questa VIP

Siemens EDA Questa® VIP integrates integrates seamlessly into advanced verification environments including testbenches built using UVM, Verilog, and VHDL. Siemens EDA, a part of Siemens Digital Industries Software, supports the leading industry-standard bus families, like PCIe, USB, and Ethernet, as well as thousands of DRAM and flash memory models. Questa VIP is the industry's only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Questa VIP for flash memory

Flash QVIP memory models offer a comprehensive solution for exhaustive verification of flash controllers, providing the flexibility to create and cover all possible verification scenarios. Flash QVIP memory models include ready-to-use verification components and easy-to-use memory APIs to increase productivity and accelerate verification signoff.

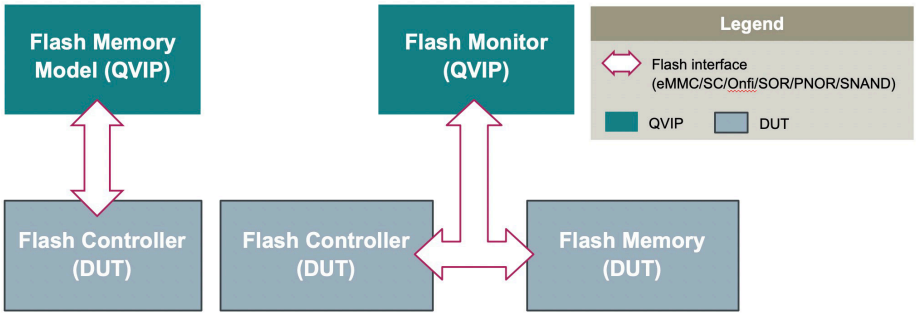


Questa QVIP

Questa Verification IP for flash memory

Flash Questa VIP memory models

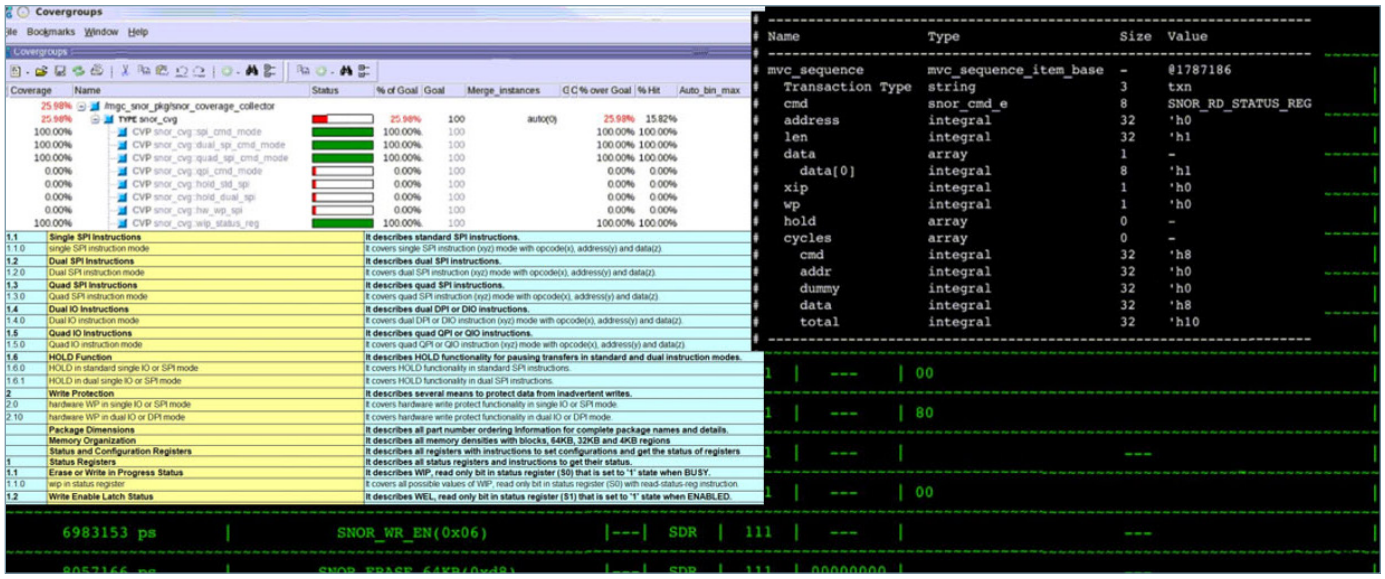
- Packaged as Verilog module
  - Multiple part number support
- Supports backdoor memory APIs
- Backdoor initialization
- Exhaustive feature support for
  - ONFI
  - SDCard/SDIO
  - eMMC
  - Serial NOR
  - Parallel NOR
  - Serial NAND
- Configurable timers using API and CSV file
- Configurable register values, user/vendor commands, instruction/command values, wait-states delay
- Byte/word memory support in parallel NOR
- SLC/TLC/MLC support in ONFI model
- Toggle NAND support in ONFI model
- Supports multi-die and multi-plane operations
- Supports CFI and SFDP standard



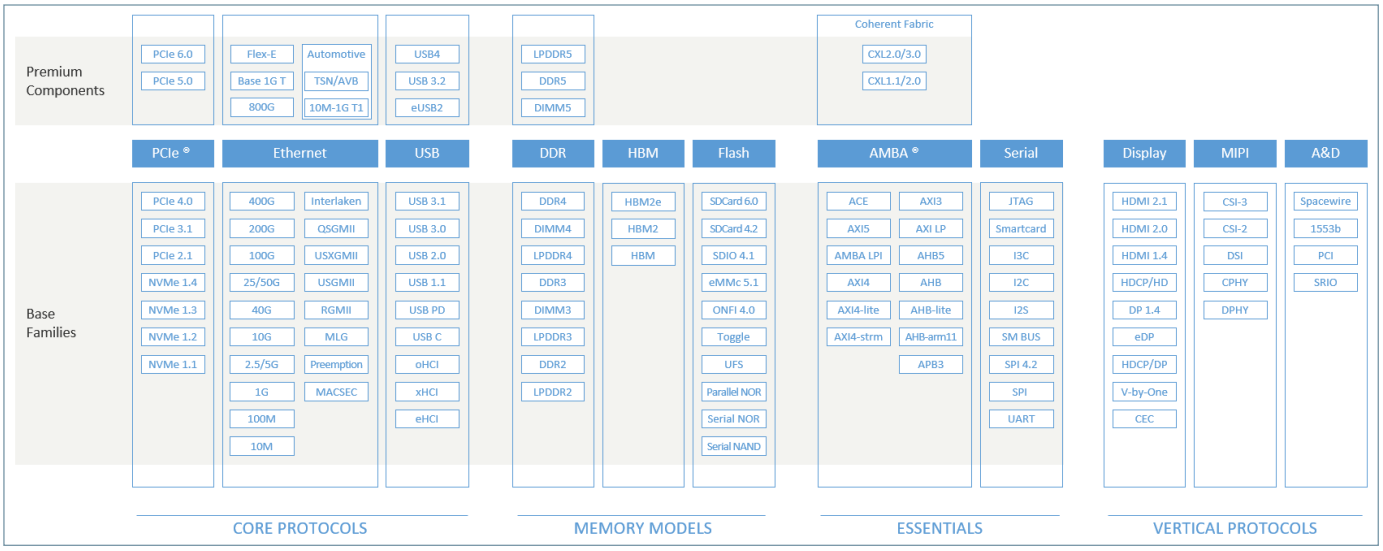
Flash QVIP Use Models

Flash Questa VIP capabilities

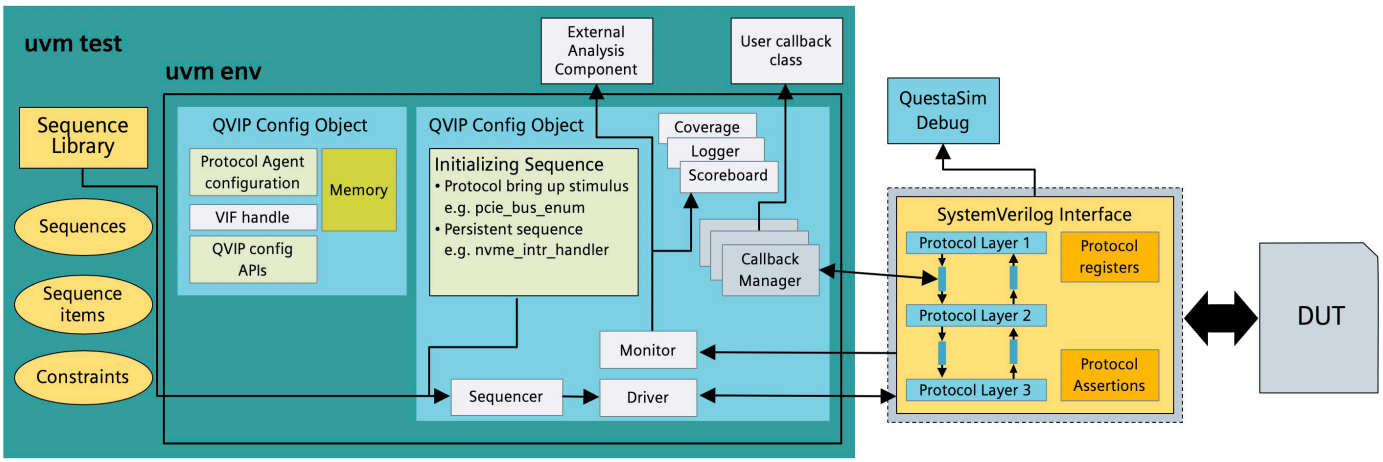
- Protocol Assertions
  - Built-in assertions analyze traffic for protocol adherence
- Coverage
  - Ready-to-use cover groups
  - Commands
  - Registers
  - Crosses for commands and possible responses
- Stimulus
  - Automatic response to commands
  - Error injection in responses
- Analysis Components
  - Listeners to print transactions in UVM format
- Loggers
  - Analysis ports for commands/instructions
  - Independent logger for each instance
  - Logs commands/responses



Questa Verification IP GUI



Questa Verification IP library



Questa VIP Testbench Arhitecture

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