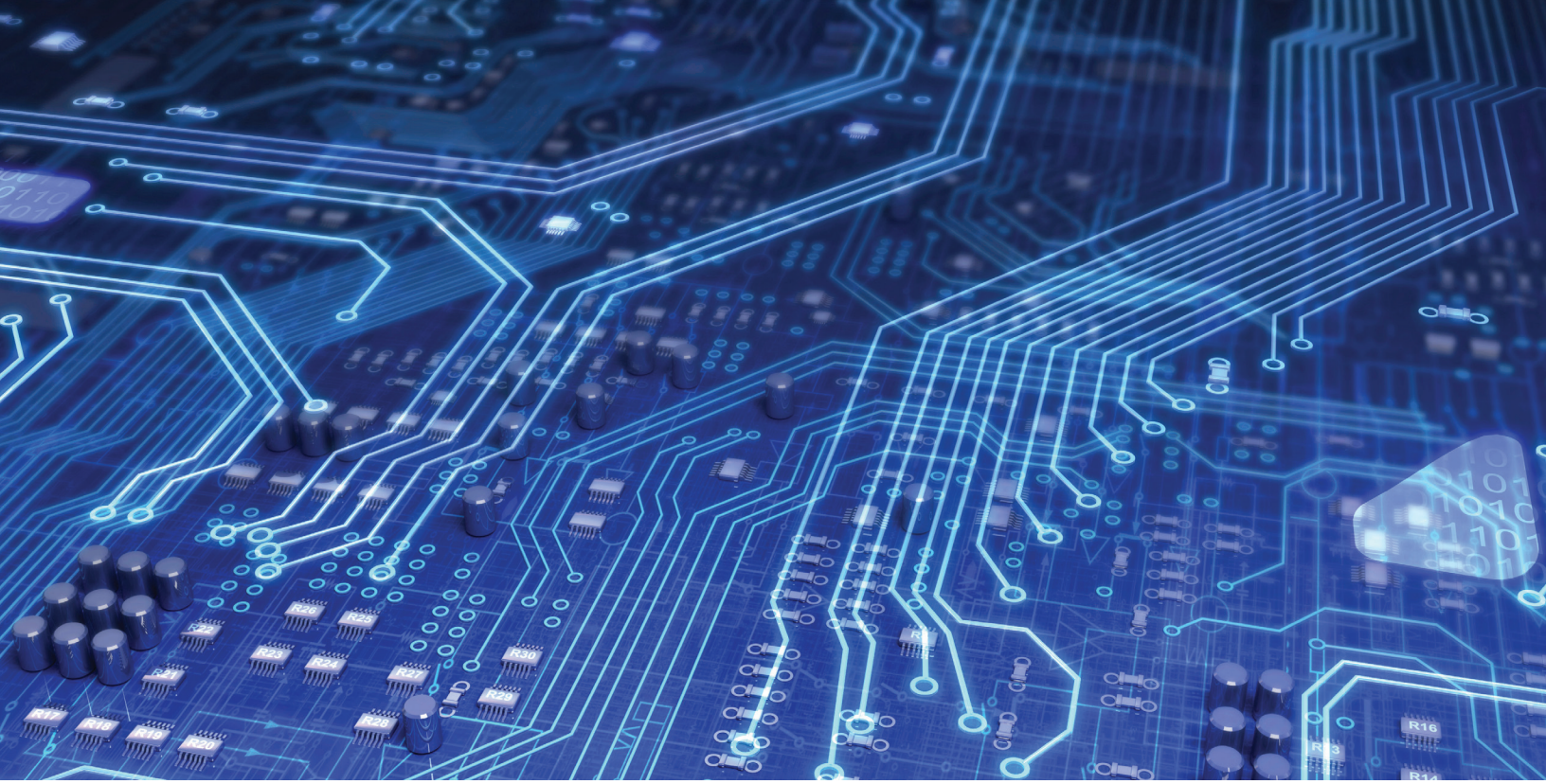

DIGITAL INDUSTRIES SOFTWARE

Why S-Parameters are superior for power module optimization

Executive summary
A power module is a high-power switching circuit – used in electric vehicles, renewable energy, photovoltaics, wind, and many more applications – that uses insulated gate bipolar transistors (IGBT) or metal-oxide-semiconductor field-effect transistors as switching elements. This paper discusses the difference in power module simulation using lumped elements and S-Parameters. Using a simple example, it is shown that S-Parameters are the better choice to predict the electrical behavior of a power module. Finally, the paper outlines a verification method suitable for automatic optimization.

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Contents

Introduction

Power modules are high-power switching circuits used in electric vehicles, renewable energy, photovoltaics, wind, and many more applications. Compared to a single device in a package, a power module packages more than one IGBT [10], MOSFET and diode together [14].

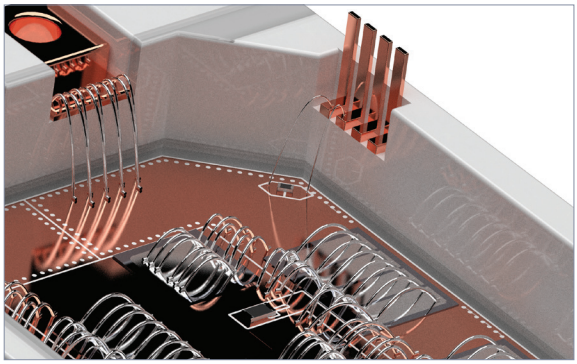

Figure 1. Power Module PI2000 Siemens EDA.

With such a multi-device package, higher voltages, currents, stable temperatures, and lower E- and H- field emissions can be achieved if the package is designed correctly. Based on these modules' high density, those characteristics become a four-dimensional design challenge, as shown in figure 2. With such a polylemma, a single power module designer can no longer predict the ripple effects of a single design change. For example, a simple change in the component placement affects all domains. The change could cause the current through all devices to no longer be distributed equally (DC behavior), and the change could also cause the switching behavior for the different devices in the module to be affected (AC behavior), already these two changes in the electrical domain led to implicit changes in thermal and EMC behavior. The goal is to achieve equal static and switching losses, to ensure equal device temperatures for all components in the package [16]. Optimized electrical behavior also leads to low EMC radiation.

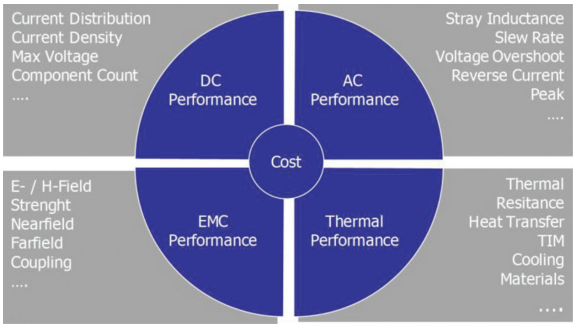

Figure 2. Power modules a four-dimensional design challenge.

Today, a high count of prototypes determines the power module design process. Personal experience shows that at least ten physical prototypes are required for one working power module fulfilling all criteria mentioned before. This is not only cost-sensitive, but it is also time-consuming. On top of this, a designer needs to consider different technology trends – device technologies like silicon, silicon-carbide and gallium-nitride [11]. Manufacturing technologies like wire bonding, component embedding, and other innovative interconnection technologies play an essential role. This paper shows how S-Parameters can be utilized to qualify and optimize power module designs. It also explains why S-Parameters were not widely used before, and the article describes an automatic solution for implementing S-Parameters in the circuit simulation.

Foundation for S-Parameter usage for power modules

Before going into the full details of S-Parameters, some basic understanding of power modules is required. A power module [4] consists, in most cases, of a single copper layer mounted directly on a ceramic substrate. This simple structure lacks a return path or reference to model a power module using a microstrip transmission line, as shown in figure 3.

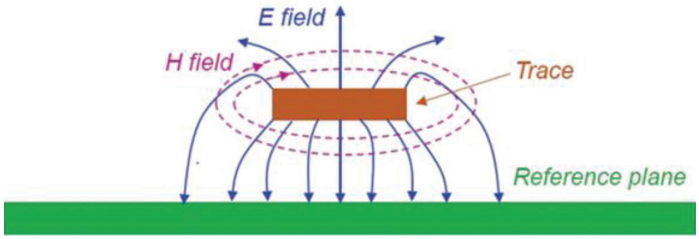

Figure 3. Microstrip line and the surrounding fields [1].

This is why an RLCG[1] parameter extraction method is currently the most common when simulating and describing power modules. Such extraction methods are widely used to extract package parasitics on ICs[2]. The equivalent circuit of a microstrip is shown in figure 4.

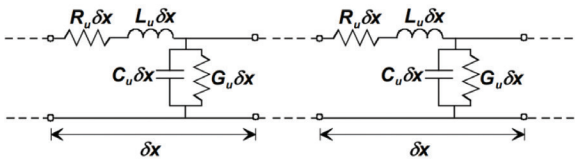

Figure 4. Microstrip line RLCG model as through representation [2].

The circuit of figure 4 must be transformed to be suitable for power modules. Instead of a through signal description, we end up with an across signal path in figure 5. This model can be further reduced by eliminating the capacitance and conductance element. We see that this method of description is suitable to describe any connection between two pins as long as we do not need to consider transmission line effects [3], such as reflection and the skin effect. This is true for small structures, small compared to the wavelength lambda, which is distributed over the copper structure.

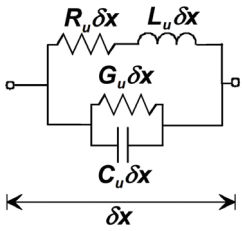

Figure 5. Microstrip line RLCG model as across representation.

The RLCG extraction allows defining a matrix of all R, L, C and G values for a given power module. For a high current path, as shown in figure 6, this is not just a single pin-to-pin connection. Instead, multiple IGBTs[3] or MOSFETs[4] are switched in parallel to share the high currents. For a matrix representation, this is, of course, no issue. Each location becomes a simulation port. These ports are marked in figure 6 with a red arrow. The most left port, J1, is used as a reference, and U1, U3 and U5 are signal ports. With this, the whole matrix can be calculated. A typical resistance matrix can be found in table 1.

1 RLCG: Resistance, Inductance, Capacitance and Conductance

2 IC: Integrated Circuits

3 IGBT: Insulated-gate bipolar transistor

4 MOSFET: Metal-oxide semiconductor field-effect transistor

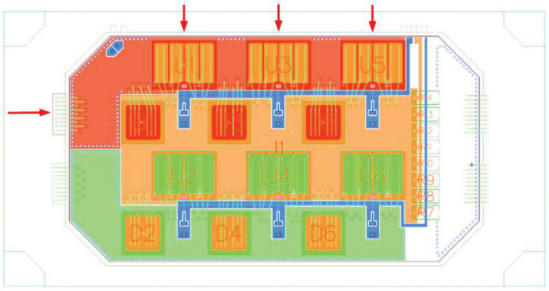

Figure 6. Power module PI2000 Siemens EDA with marked ports.

R-Matrix	**U1**	**U3**	**U5**
U1	R_{U1-J1}	R_{U1-U3}	R_{U1-U5}
U3	R_{U3-U1}	R_{U3-J1}	R_{U3-U5}
U5	R_{U5-U1}	R_{U5-U3}	R_{U5-J1}

Table 1. R-Matrix for VPP net of the PI2000 power module with J1 as reference.

The table must be implemented in a SPICE netlist for a circuit simulation. The transformation of the matrix to a SPICE circuit makes things difficult. A general rule is that the SPICE circuit must be composed in the direction of the electrical current. If J1 is the enclosure terminal of the power module, the current flow direction is from the IGBT U1 to J1, from U3 to J1 and from U5 to J1. These values can be found on the main diagonal of table 1. A SPICE netlist could look like this:

```
.subckt RMatrix J1 U1 U3 U5
RU1J1 U1 J1 {VALUE_RU1J1}
RU3J1 U3 J1 {VALUE_RU3J1}
RU5J1 U5 J1 {VALUE_RU5J1}
.ends
```

Circuit 1. SPICE circuit of the main diagonal of the R-matrix.

This example shows that the selection of the reference pin has a huge impact on the final result. Changing the reference pin from J1 to U3 demonstrates the behavior in more detail:

R-Matrix	**U1**	**J1**	**U5**
U1	R_{U1-U3}	R_{U1-J1}	R_{U1-U5}
J1	R_{J1-U1}	R_{J1-U3}	R_{J1-U5}
U5	R_{U5-U1}	R_{U5-J1}	R_{U5-U3}

Table 2. R-Matrix for VPP net of the PI2000 power module with U3 as reference.

For the composed SPICE netlist, the resistance from J1 to U1 changed from R_{U1-J1} to $R_{J1-U3} + R_{U1-U3}$. This is not correct. Engineers must carefully pick reference pins in a power module verification scenario to achieve the most accurate simulation result. It is shown later that the SPICE representation has other disadvantages in the simulation performance and broadband accuracy.

Another way to model the connection between two or more circuit nodes is using scattering parameters or S-Parameters in a short form. S-Parameters are widely used to analyze high-speed interfaces such as PCIe[5] or Ethernet. Based on [2],[3], an S-Parameter or an S-matrix is a mathematical concept to describe wave propagation through a multi-port network. In this definition, already one advantage and one disadvantage can be found. The advantage is that S-Parameters are capable of handling multi- port electrical networks. The disadvantage is wave propagation. Power modules based on silicon IGBTs switching frequency are far below 1 MHz. Even if harmonic frequencies are considered, it is hard to argue that wave propagation is required. Typical power modules in a performance range of 1700V and 750A, such as the Infineon FF750R17ME7D, has substrate dimension of 38mm x 100mm [4]. The wavelength of a 1 MHz signal is much bigger than this geometrical structure. Eq. (1) shows that considering a dielectric constant of a typical power module substrate such as AlN,[6] the wavelength is 99.93 m. An RLCG representation would be sufficient to characterize a power module based on Si devices.

[5] PCIe: Peripheral component interconnect express

[6] AlN: Aluminium Nitride

Looking into the future, WBG[7] semiconductors such as SiC[8] and GaN[9] [11] are moving fast forward. These new technologies also have much higher switching frequencies and will introduce the demand for full wave effects.

$$\lambda_{Sub} = \frac{c_{Mat}}{f_{Sig}} = \frac{\frac{c}{\sqrt{\varepsilon}}}{1\ MHz} = \frac{\frac{c}{\sqrt{9}}}{1\ MHz} = 99.93\ m \quad \text{Eq. (1)}$$

There are two challenges in combination with S-Parameter simulation. Similar to the description of the microstrip, the industry used to have a reference net for each signal. As mentioned before, for power modules, this is not the case.

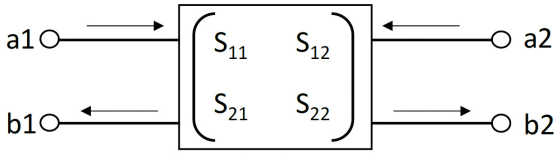

Figure 7. Two-Port network represented as S-Parameter with reference net b and signal net a.

Figure 7 shows a two-port network. On the left side, there is pin a1 and b1, where a1 is the signal pin, and b1 is the reference pin. The same pattern can be applied to the right side. Figure 7 must be transformed for power modules to consider the missing reference net. Figure 8 shows the result of the conversion. A pin of the signal net is used as a reference pin. This also represents the method which applies to power modules.

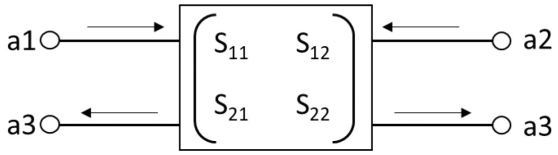

Figure 8. Two-Port network without reference net.

Without the work described in this paper, the transformed S-Parameter cannot be simulated in a circuit simulator. The reason for this is that due to the standardization for high-speed applications, all reference pins are not exported, and the pin is assumed to be connected to the reference. In the case of high-speed PCBs[10], this is ground or net 0. Compared to the desired situation in figure 8, the simplification is shown in figure 9. This means that with the current solution, the pin a3 does not exist in the S-Parameter. Still, it does exist for the circuit simulator. If the S-Parameter file gets back annotated to the circuit simulation, pin a3 is disconnected.

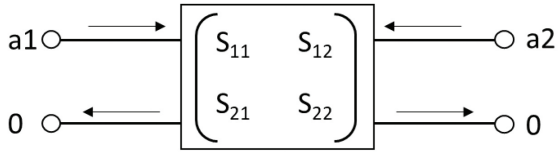

Figure 9. Simplified two-port network model used today.

This paper solves this problem and enables the usage of S-Parameters in circuit simulators like Xpedition AMS[11] from Siemens. It also outlines the capabilities of the S-Parameter for optimization, for example, using a power module compliant check based on an S-Parameter. This paper does not describe how the DC behavior for S-Parameters is optimized. Modern solvers like Xpedition AMS have integrated interpolation methods to handle DC operation points.

7 WBG: Wide Band Gap

8 SiC: Silicon Carbide

9 GaN: Galium Nitrid

10 PCB: Printed circuit board

11 Xpedition AMS: Analogue, mixed-signal circuit simulator based on the printed circuit board and substrate design suite Xpedition from Siemens

Solution to missing reference pins

The solution is demonstrated in the example in figure 6 for the positive supply voltage called net VPP. For the simulation of the S-Parameter and the later used RLCG matrix, HyperLynx Advanced Solvers, such as Fast 3D and the Hybrid solver, are used [5,20].

Ports	Net	Pin	Ref. Net	Ref. Pin
1 (U1)	VPP	$U1_C$	VPP	$J1_P$
2 (U3)	VPP	$U3_C$	VPP	$J1_P$
3 (U5)	VPP	$U5_C$	VPP	$J1_P$

Table 3. Detailed port definition of the net VPP.

To reproduce the simulation results, the following mesh and solver settings were used:

- Mesh frequency: 5 GHz with ten cells per wavelength
- S-Parameter port extraction from 10kHz to 1 GHz with 301 frequency points
- Reference channel resistance 0.1 Ω

The simulation result shown in figure 10 was expected. For a frequency between 10 kHz to approximately 1 MHz, the ohms resistance of the copper is dominant at higher frequencies, the inductance path becomes dominant until 10 MHz. After that, a resistive part takes over. This behavior reminds us of figure 5. Over 100 MHz, we see additional losses, but, overall, this shows that the RLCG representation has a good fit, at least between 10 kHz and 1 GHz. The component placement of U1, U3 and U5 in relation to J1 can explain the S-Parameter order in figure 10. Figure 6 shows that the distance between U1 and J1 is the shortest and the distance between U5 and J1 is the longest. For this reason, it is not surprising that S11 (red) have the lowest attenuation and S33 has the highest attenuation.

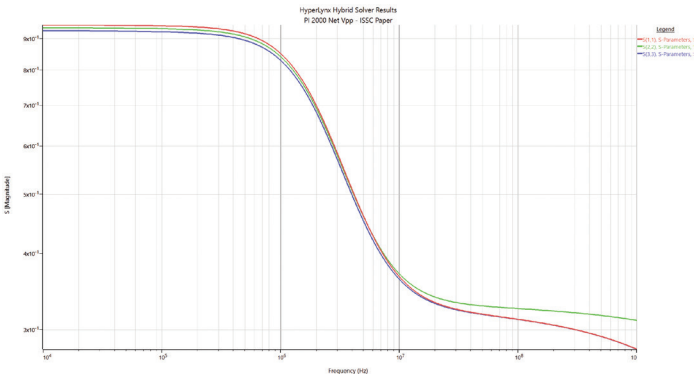

Figure 10. HyperLynx Hybrid Solver simulation results for net VPP.

The advantage of an S-Parameter in a circuit simulation is that no transformation into a SPICE netlist is required. Compared to the RLGC, there is not only a representation of the main diagonal. Instead, the full S-matrix is available. This is important to automate the process since it is no longer required to have detailed knowledge about current paths, which was needed to select the reference pin. A SPICE wrapper file must be generated to use S-Parameters in Xpedition AMS. Line 4 in circuit 2 shows all available pins of the SPICE subcircuit. In this line, currently, J1-P, the reference pin of table 3 is missing. In line 12, all signal and reference pins are shown. Each pin is bundled as predicted with pin 0 and not with the actual reference pin. To transform the wrapper according to figure 8, the wrapper file needs to get enhanced by the reference pin in lines 4 and 12.

```
1.  * Wilfried Wessel TU Dublin
2.  * Wrapper circuit for S parameter
3.  .subckt wrapper_PI2000_VPP_ISSC_Paper
4.  + U1-C U3-C U5-C
5.  .model Fblock macro lang=c
6.  + YSPARAM FBLOCK param :
7.  + idx_m = 0
8.  + EXTRAP_TO_DC = 1
9.  + FORCE_PASSIVITY = 2
10. + SYMMETRY = 1
11. + POLE_REDUCTION = 0
12. + pin : U1-C 0 U3-C 0 U5-C 0
13. + STRING : 'PI2000_VPP_ISSC_Paper.s3p'
14. .ends wrapper_PI2000_VPP_ISSC_Paper
```

Circuit 2. Standard S-Parameter wrapper file.

A subset of the transformed wrapper file is shown in circuit 3. All required changes are marked in yellow. For a small example like this, this process is straight-forward and can help to define all requirements for an automated version.

Since the SPICE wrapper contains no information about the reference pin or pins, another source must be found. In line 13 of circuit 2, the S-Parameter file is linked to the wrapper file. Based on the author's work for parasitic extraction and back annotation in 2012 [6], the header information of each S-Parameter exported by any HyperLynx product was enhanced to contain all required information. The port information is marked in circuit 4 in yellow. Both files are ASCII[12] files, and at least for the Siemens software environment, the information in the S-Parameter header is standardized. This is the foundation for the full automation of this process.

```
3…
4.  + U1-C U3-C U5-C J1-C
11…
12. + pin : U1-C J1-C U3-C J1-C U5-C
J1-C
```

Circuit 3. Enhanced S-Parameter wrapper file.

```
! Touchstone file written by Hybrid
  Solver VX.2.13
! 2023/03/21, 05:05:30 PM
! HyperLynx Advanced Solvers
! Project: PI2000_VPP_ISSC_Paper
! Simulation: PI2000_VPP_ISSC_Paper
! User: wwessel
! Computer: DEM-WWESSEL-WX

! Single-ended S-parameters
! HL_PORTMAP 1.0
! PORT 1 +(PIN U1.C, VPP, P) -(PIN
  J1.P, VPP, P) NAME:VPP.U1.VPP
! PORT 2 +(PIN U3.C, VPP, P) -(PIN
  J1.P, VPP, P) NAME:VPP.U3.VPP
! PORT 3 +(PIN U5.C, VPP, P) -(PIN
  J1.P, VPP, P) NAME:VPP.U5.VPP
! CONNECT 1, 2, 3;
! END_HL_PORTMAP
```

Circuit 4. S-Parameter header information.

[12] ASCII: American Standard Code for Information Interchange

Full automatic SPICE wrapper transformation

In [3] it was described how an S-Parameter wrapper could be transformed manually. These single steps can now be implemented in code; several options are available. For a direct integration into the Siemens power modules design suite, Xpedition VB.Net is recommended. VB.Net is a flexible, object-based, powerful programming language well-suited for developing customizations based on COM APIs, such as Xpedition.

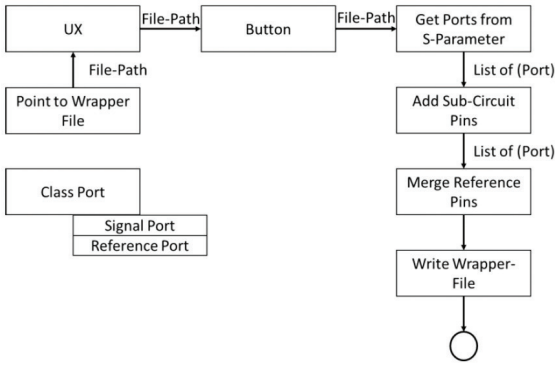

Figure 11. VB.Net power module S-Parameter merger.

Before implementing functionality, a new class with two items was defined. In figure 11, the class is called “Port.” This class has two elements a signal and a reference port. This technique helps to use VB.Net embedded list functions. If the overhead for the user interface is ignored, the implementation has four functions: get ports, add sub-circuit pins, merge reference pins, and the function to write a new wrapper file. In the “Get Ports from the S-Parameter” function, the S-Parameter file handed over from the user interface is parsed, and all port pairs are stored in a list of the class “Port.” This sort of dictionary format is required since multiple nets, and reference pins are possible. With the complete port information available, the function “Add Sub-Circuit Pins” adds the missing pins sub-circuit pins, as was shown in line 4 when transformed from circuit 2 to circuit 3. For this function VB.Net has a filter function available which is called “Distinct.” This function is applied to avoid duplicated pins in the sub-circuit header. The function “Merge Reference Pins” of figure 11 replaces all 0 in line 12 of circuit 2 with the correct reference pin. A new wrapper file is generated at the end of the merge process, which can be used without manual intervention.

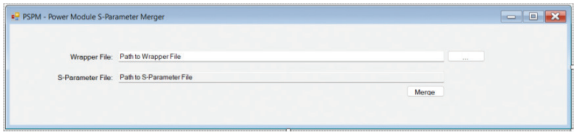

Figure 12. User interface of the power module S-Parameter merger.

The easy-to-use user interface has only two buttons, one to point to the SPICE wrapper file and another button called “Merge” to start the fully automatic merge process. The application can be directly embedded into Xpedition, allowing the engineer to seamlessly integrate the whole power module verification process. Additional benefits and a functions test will be described in the next section.

Function test

The function test is done with the whole power module shown in figure 6. For this reason, a complete SPICE simulation in Xpedition AMS was configured. The circuit is represented below. The circuit shows three parallel IGBTs and freewheeling diodes for the high-site path and three parallel IGBTs and free-wheeling diodes for the low-site path. This is a typical optimization use case where design engineers want to achieve equal static and dynamic switching losses for each device. This translates into equivalent resistance and inductance behavior for electrical parameters for each device. Optimizing these parameters helps to ensure device temperatures are similar [16]. This is important for an extended power module life cycle and reliability.

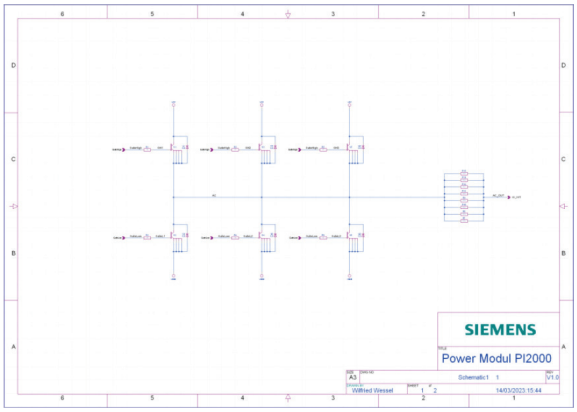

Figure 13. PI2000 schematic Siemens EDA

The power module was designed with Si IGBTs of Infineon IGC193T120 [7] since they are still widely used and have a better price/performance ratio than SiC or GaN due to the established manufacturing process. The simulation is performed three times, first without any parasitic behavior, second using the SPICE parasitics composed by the RLCG matrix as described above, and the third simulation using S-Parameters. The simulation result is analyzed for static DC behavior, stray inductance [18] and simulation performance measured by time.

Figure 14 shows the emitter current through the IGBT U1, U3 and U5. The current through U1 with 76.46 A is approximately 14.5 A higher than the current through the two other devices. This leads to the static switching phase to a much higher self-heating. Referring to table 4, there are minor differences in the DC path. As described before, the S-Parameter requires wave signal propagation, so the DC point must be calculated by interpolation. This is not the case for the RLCG representation. The result shows that these differences are so minor that they are still suitable for optimizing the DC path.

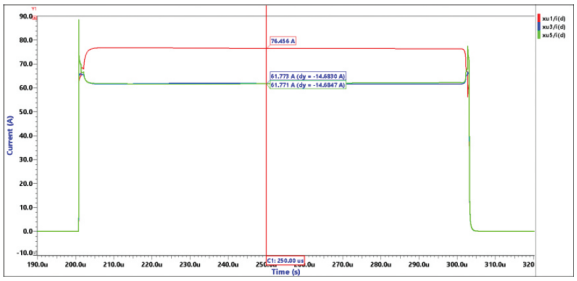

Figure 14. Currents through U1 (red), U3 (blue), and U5 (green) using S-Parameter.

For the description of higher frequency switching behavior S-Parameters are superior. Figure 15 shows the collector-emitter voltage and the derivate of the emitter current during the IGBT switch-off phase. These values can be used to calculate the stray inductance each device sees. It can be identified in figure 15 that the voltage overshoot is similar (25.6 V) for all IGBT devices. The derivate of the emitter current shows some differences. This leads to a stray inductance [18] of 18.62 nH for U1 and 15.22 nH for U5. For the S-Parameter representation, the difference is not as high as the difference using SPICE parasitics, with 35.34 nH for U1 and 21.14 nH for U5. There are two main reasons for the difference. The first reason is the better high-frequency accuracy of the S-Parameter. The second reason is due to the high node and device count of the SPICE

parasitic. This causes excessive ringing effects, and the stray inductance results strongly depend on the simulation time step. The ringing also creates difficulties measuring at the correct time location. Minor differences in time have huge effects on the stray inductance.

The function test proved that the automatic S-Parameter wrapper generation works correctly. Table 4 shows a huge benefit in switching accuracy and a performance enhancement by approximately 20. The result is essential for holistic and fully automated power module optimization, described further in the next section.

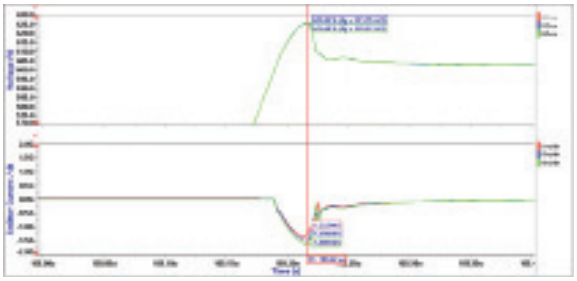

Figure 15. Top emitter-collector voltage with an overshoot of U1 (red), U3 (blue), and U5 (green). Bottom derivative of the emitter current of U1 (red), U3 (blue), and U5 (green) using S-Parameter.

	Ideal simulation	SPICE parasitics	S-Parameter
Current through for U1/U3/U5	66.66 A / 66.66 A 66.66 A	81.39 A / 59.37 A 59.24 A	76.46 A / 61.77 A 61.77 A
Stray inductance for U1/U3/U5	0 nH / 0 nH / 0 nH	35.34 nH / 25.80 nH 21.14 nH	18.62 nH / 17.11 nH 15.22 nH
Nodes/Devices	230 / 390	667 / 6583	290 /391
Performance	8 sec.	19 min. 53 sec.	1 min. 11 sec.

Table 4. Simulation summary.

S-Parameter compliance check and optimization

The work of the paper enabled the usage of an S-Parameter for time domain simulation. However, table 4 shows that the simulation with the S-Parameter still takes ten times longer than without any board or substrate parasitics. For this reason, it is recommended to use an S-Parameter compliance check before going into the functional simulation. This kind of compliance check does not exist for power modules, but the method can be borrowed from high-speed SERDES analysis [7]. For the SERDES interface, the compliance check verifies if a board conforms to a certain standard, such as PCIe 4.0. Instead of full-time domain analysis, everything is modeled with S-Parameters and compared against worst-case conditions to meet the standard requirements. For power modules, these requirements are not available. Based on the performance figures of a power module, typical values can be extracted as lumped values, such as the stray inductance must not exceed 20 nH or the copper resistance from input to output must not exceed 200 µΩ. These values are for a single current path through one IGBT and are decreased by switching multiple IGBTs in parallel. To generate a reference S-Parameter, a typical reference circuit was needed.

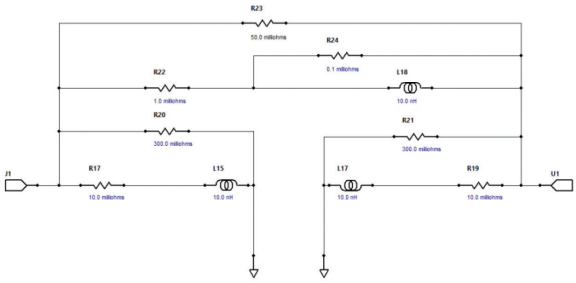

Figure 16. Simple circuit to create reference S-Parameter.

The circuit to generate the reference S-Parameter was developed based on figure 4 and with empiric experiments figure 16. In our example, R17 and L15 can set up the resistance and the inductance path. Tools such as HyperLynx LineSim can quickly generate the S-Parameter of this structure. This process can also be fully automated using Python.

After adjusting the parameters in the circuit and including all S-Parameters in the same plot, it can be verified if the general parameters were exceeded. In figure 17, no other S-Parameter crosses or undershoots the reference S-Parameter (pink). This means without any further simulation; it can be guaranteed that the basic parameters are sufficient regarding the absolute values. The values are in the so-called high confidence region.

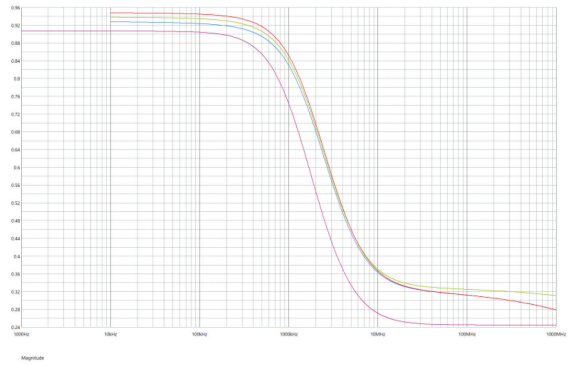

Figure 17. Power module S-Parameter compliance check example S11 (red) U1-J1, S22 (green) U3-J1, S33 (blue) U5-U1, and the reference S-Parameter (pink).

The same technique can also be used to verify if the relative values are suitable. A lower and an upper S-Parameter limit is generated for this use case. The example in figure 18 shows that the deviation of the resistance value between U1, U3, and U5 is too big. This finding can now be used to optimize the placement in a very early verification phase. A similar approach can be applied to the inductance value.

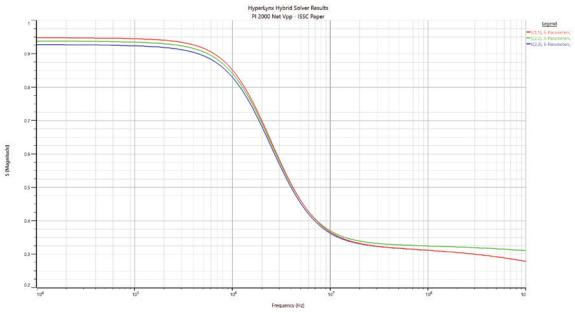

Figure 18. Power module S-Parameter compliance check example S11 (red) U1-J1, S22 (green) U3-J1, S33 (blue) U5-U1, and the reference S-Parameter (pink).

The desired workflow in the future aims for full automation. Currently, single parameters are analyzed to see if optimization is possible and to validate the order of changes. To optimize the resistance behavior, a power module designer has two choices. The placement of the IGBTs can be changed, or the copper/bond wire connection.

In the first test, the single IGBT (U1) was moved in a positive x direction (green arrow in figure 19) without changing any copper structures.

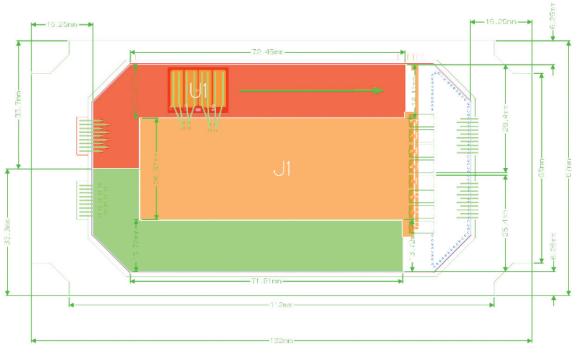

Figure 19. Effect of IGBT positions on electrical resistance.

Figure 20 shows a linear resistance increase if the IGBT is moved along the x-axis. This means in the current power module implementation it is not possible to adjust the placement so that all S-Parameters are matching relative to each other. This is an important finding. Currently, engineers and companies are asking heavily for automatic optimization. This simple example shows that optimization parameters are highly dependent on the implementation.

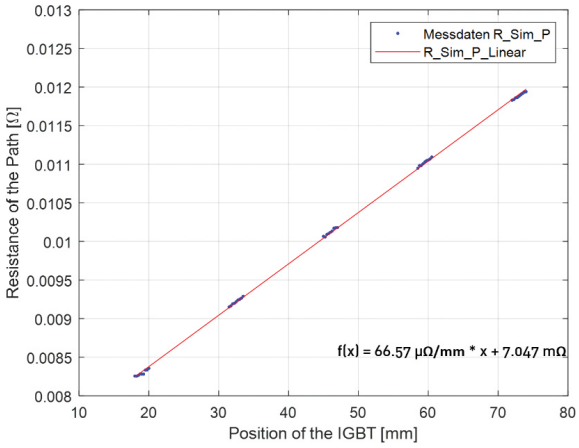

Figure 20. Resistance based on the position of IGBT U1.

In another example, a copper change is introduced. In most cases, a designer is limited in the degree of freedom based on the mechanical structure. For this reason, the second example only shows a minor copper chance be implementing corner radii. In the current implementation, this chance can decrease the overall electrical resistance path but is insufficient to fine-tune each IGBT individual figure 22.

For this reason, methods like copper trimming with obstructs and changing the number of wire bonds and other dynamic ways must be used. This method will require automatic optimization methods.

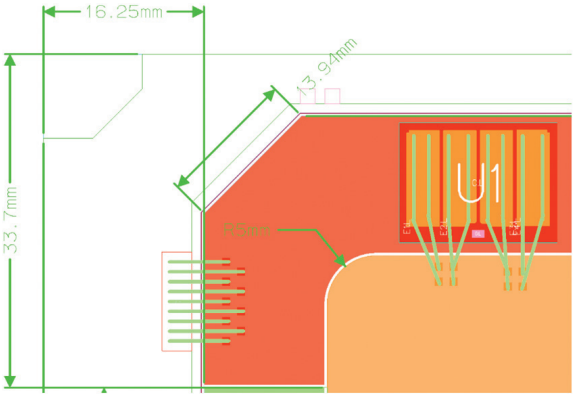

Figure 21. Power module optimization by introducing corner radii.

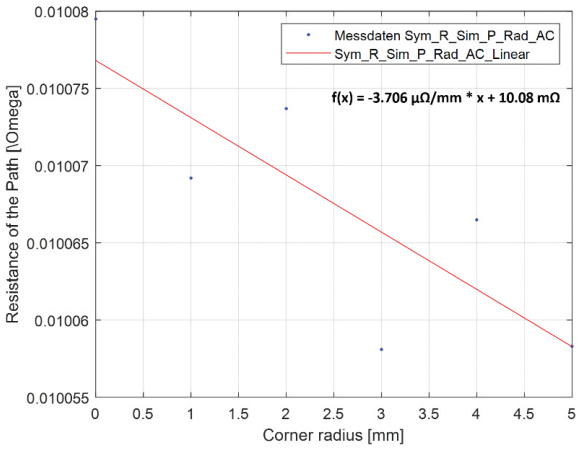

Figure 22. Simulated resistance with various corner radii.

Conclusion

For a fully automated and holistic optimization approach of power modules, relying on a single source of truth is essential. Lumped parasitics as SPICE subcircuits were used before to perform time domain functional simulation for power modules. The main reason was the missing reference plane or return current structures. Only view references like [8] were found using S-Parameters in this area. Table 3 showed some advantages of using an S-Parameter in the functional simulation. These advantages were increased simulation performance by factor 20 and increased high-speed accuracy.

Other advantages are that the simulation result no longer depends on the engineer's experience setting up the reference pin. The work of the paper enables the use of S-Parameters in the time domain analysis. It was demonstrated that future optimization methods in the electronic domain could be performed in two steps: in the first step of the process, the power module S-Parameters are compared to reference S-Parameters. In the second step, the same set of S-Parameters is used to perform and analyze the transient time domain behavior. Currently, there is no industry standard to specify power modules with S-Parameters.

For this reason, the reference parameters are generated based on typical requirements for stray inductance and resistance. This makes it easy for the engineer or optimization algorithm to analyze if all simulated parameters are in the high confidence region. This verification method in the first step is borrowed from high-speed SERDES analysis and is called a compliance check.

The main advantage is that the same set of S-Parameters can be used to perform the time domain simulation. This guarantees data integrity and that a fully automated process does not try to fix or optimize issues caused by transforming an RLCG matrix into a SPICE netlist, as described above. The paper shows that the solution can be easily integrated into the engineers working environment using a VB.Net application. This and the fact that, for example, all Siemens EDA products have an API available, allows us to develop a complete optimization.

In the last section of the paper, we also saw that not all chances, e.g., placement chances or copper chances, are suitable to optimize the power module for equality in static and dynamic losses, which is essential for similar thermal behavior. This is why single change parameters must be studied and documented further. In the future, these parameters are also no longer limited to the time and frequency domain; the parameters must also be analyzed in the thermal and mechanic domain. An example is thermal resistance and thermal stress. Future research will end up with a set of rules to be verified using design rule checks. Before the optimization process, this set ensures a good entry point, the ability to optimize, and reduced time to result.

This enables us to provide design methods and a solution to withstand the high demand for new efficient power modules in the future.

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