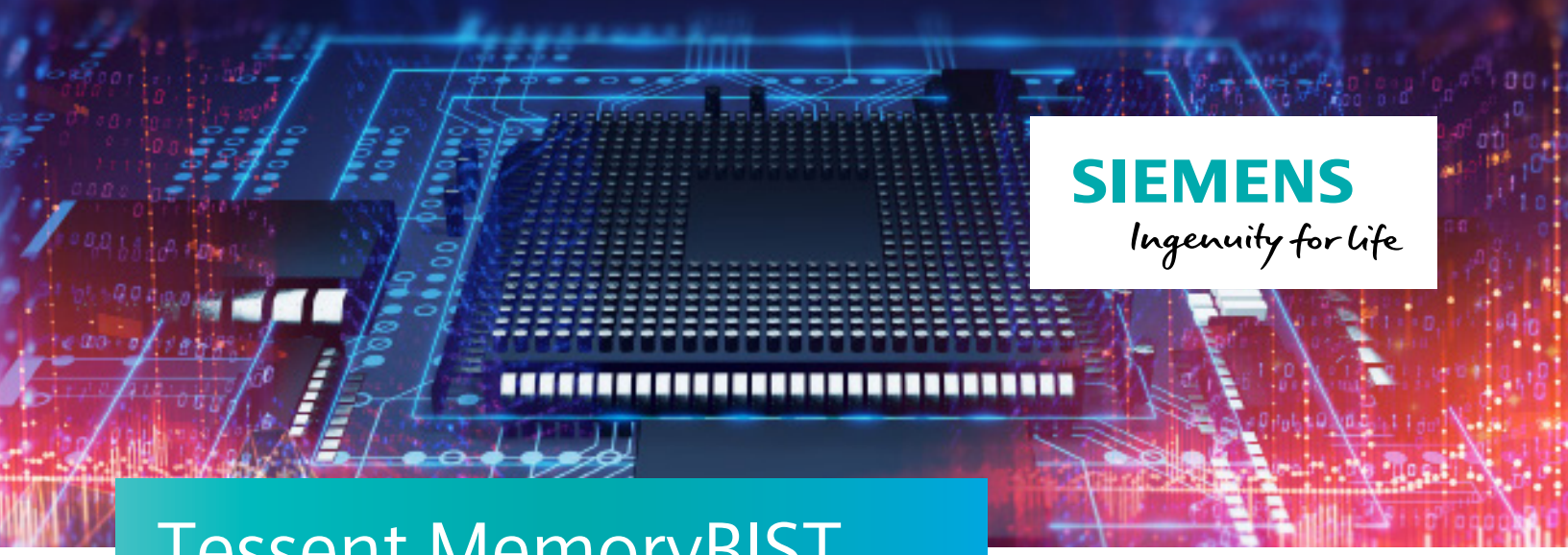


SIEMENS
Ingenuity for life

Tessent MemoryBIST

Embedded memory self-test, repair, and debug

Benefits

- Flexible and automated BIST IP integration, access network integration, and pattern validation shortens time-to-market.
- Resource sharing and flow integration with Tessent Logic BIST and Tessent TestKompress reduces overall DFT cost and increases defect coverage.
- Design-time and field programmable algorithm specification allows full control of test quality and test time trade-offs.
- User controllable area and test time trade-off options enables product specific test cost optimization.
- On-chip global eFuse management reduces overall manufacturing costs.
- Desktop-based test debug and characterization speeds time-to-market.

Features

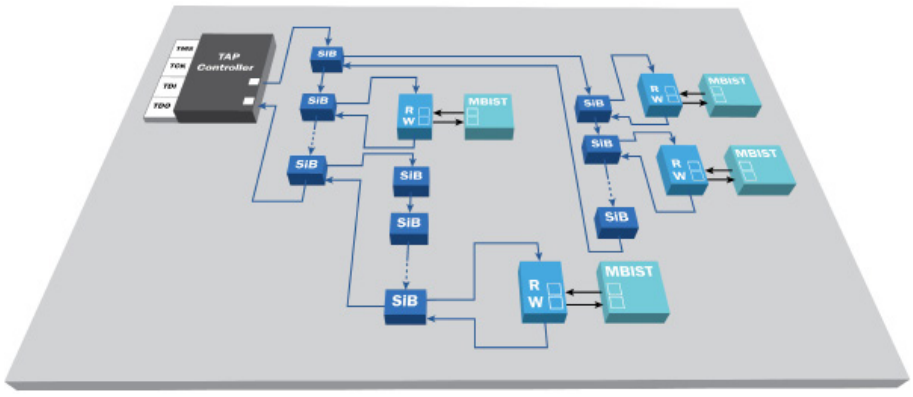
- Hard and soft programmable algorithm support to balance quality and test time.
- Comprehensive defect coverage for advanced technologies such as FinFET.
- Power-aware test and repair for multiple power domains.
- Fully autonomous hard and soft incremental repair solution for on-chip and off-chip analysis.

Industry-leading solution for Memory Built-In Self-Test

The Tessent™ MemoryBIST software and IP provides a complete solution for at-speed test, diagnosis, repair, debug, and characterization of embedded memories. The solution's architecture is hierarchical, allowing built-in self-test and self-repair capabilities to be added to individual cores as well as at the top level.

On-chip generated test patterns are delivered to the memories at application clock frequencies. The Tessent MemoryBIST controllers are configurable to support a variety of memory types, as well as a range of memory timing interfaces and memory port configurations. The controllers are accessed and controlled through an IEEE 1687-2014 (IJTAG) network. This highly configurable network is used to access all Tessent IP and can support any 3rd party IJTAG-compliant instruments. The controllers can be accessed throughout the life of the integrated circuit, including manufacturing test, silicon debug, and in-system test.

Tessent MemoryBIST includes a comprehensive and flexible implementation flow built on the Tessent Shell platform. Automation is provided for design rule checking, test planning, BIST integration, and verification either on the RTL or at the gate level. The back-end flow for memory test (debug and characterization) is managed by Tessent SiliconInsight™, an interactive, desktop-based debug environment, which can provide diagnosis data down to the chip-level XY coordinate of failing cells.



Hierarchical Tessent MemoryBIST infrastructure.

Tessent MemoryBIST

Features *continued*

- Advanced BIST Access Port (BAP) configurable interface for minimal latency in-system test and reduced ATE test time.
- External memory and 2.5/3D-IC support for multi-die and TSV interconnects.
- Shared-bus interface and full interoperability with 3rd party memory IP.
- Unified characterization and debug platform with Tessent SiliconInsight.

Advanced BIST Access Port

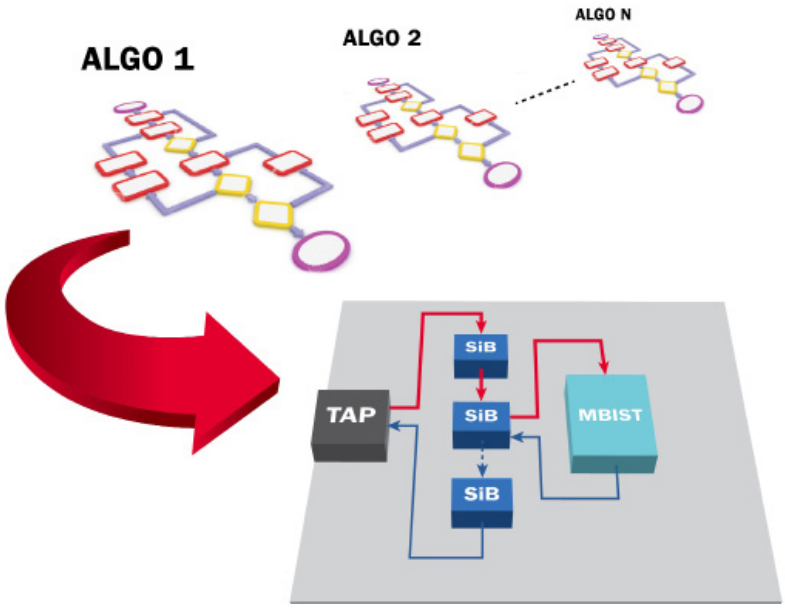
The advanced BAP provides a configurable interface to enable optimized in-system testing. This direct access interface supports a low-latency protocol to configure the MemoryBIST controller, execute Go/NoGo tests, and monitor the pass/fail status. Test time can be significantly reduced by eliminating shift cycles to serially configure the controllers in the IJTAG environment.

Algorithm programmability

At design time, memory test algorithms can be hard-coded into the Tessent MemoryBIST controller. The algorithms can be chosen from a comprehensive library collection or customized by the user. Any of these algorithms can then be applied to each memory through run-time control. This capability is useful for optimizing test time by selecting shorter test algorithms as the manufacturing process matures.

In addition, the Tessent MemoryBIST Field Programmable option allows any memory BIST controller to include full run-time programmability. With this feature, any user-programmed memory test algorithm can be downloaded into the BIST controller while on the tester or in-system.

This capability allows unforeseen defect mechanisms to be handled without requiring a design re-spin. Field algorithm programming facilitates yield learning because different diagnostic algorithms can be downloaded during yield ramp, as needed.



Tessent MemoryBIST field programmability.

Power-Aware On-Chip Self-Repair

The Tessent MemoryBIST repair option eliminates the complexities and costs associated with external repair flows. It tests and permanently repairs all defective memories in a chip using virtually no external resources. The Tessent MemoryBIST built-in self-repair (BISR) architecture uses programmable fuses (eFuses) to store memory repair info. During memory test, built-in repair analysis engines within each BIST controller calculate the fuse information needed to repair each memory.

Fuse information can be accumulated over different test conditions. The final data is stored in a local BISR register, which is part of a single serial chain specific to a power domain. These serial chains are operated by a fuse controller to shift and compress repair data into a central eFuse array.

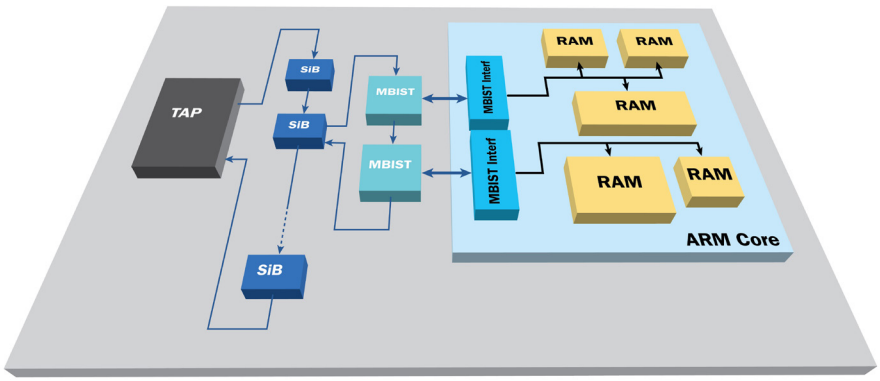
Hard incremental repair is also supported. The results of the additional repair analysis performed during subsequent manufacturing or in-system tests can be added to the stored fuse information.

Tessent MemoryBIST offers flexibility for eFuse management to help balance test time and routing congestion. With a central eFuse, a single serial chain can be used to minimize routing. With distributed eFuses across cores, parallel broadcast can be used to minimize overall repair time.

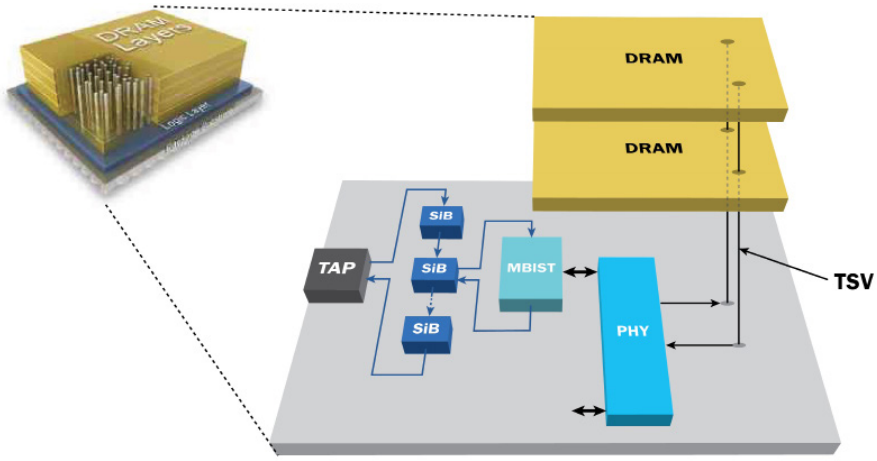
Shared-bus interface support

Processor cores from vendors such as Arm® can provide a shared-bus interface to the memories internal to the processor core IP. This interface provides a standard set of address, data, and control ports to access all memories embedded within each processor core. The memory BIST controller no longer communicates directly to each memory but must now understand how to gain access to each memory through the common interface signals. In addition, it must account for the different levels of pipelining to and from each memory.

Tessent MemoryBIST supports the integration of memory BIST and repair capabilities into a design that contains both stand-alone memories and memories embedded within an IP core that are only accessible through a shared-bus interface.



Testing through a shared-bus interface.



Testing 3D stacked memory die.

External memory and 3D-IC support

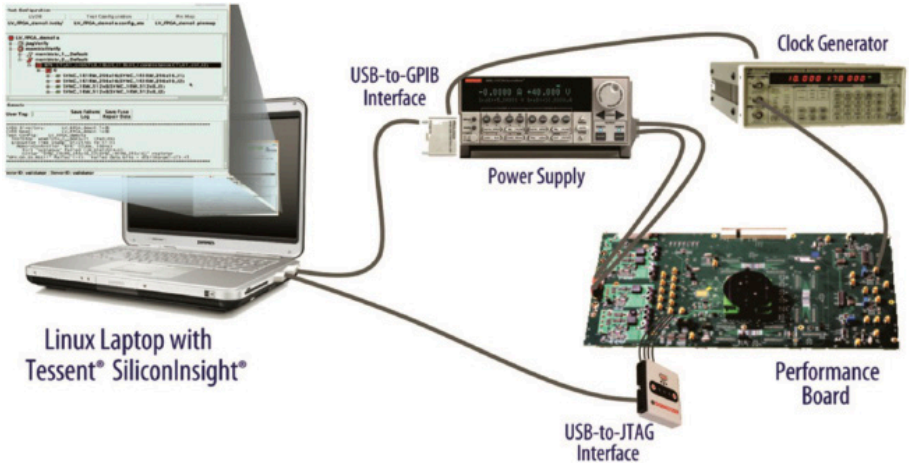
Tessent MemoryBIST provides support for testing memories that are external to the device containing the BIST IP. Support is provided for both stand-alone memory packages at the board-level and for 2.5/3D packages consisting of one or more memory die stacked on top of a separate logic die.

The memory BIST control logic is integrated into the logic chip allowing at-speed testing of the memory bus logic and connections. Tessent MemoryBIST supports Wide IO and HBM interfaces as well as package configurations where multiple memory die are stacked and connected to a single logic die via the same electrical interconnects. Both bond wire and through- silicon via (TSV)-based interconnects can be tested. The field programmability option supports changes in the memory die, or variant stacks that use different memory designs.

Test Debug and Characterization

Tessent SiliconInsight provides an automated environment for test bring-up, debug, and silicon characterization. Designers can interactively execute tests, collect data, and generate shmoo plots for any selection and order of BIST-tested blocks on the device, either in a lab environment or on the tester through ATE-Connect™. ATE-Connect enables direct communication between Tessent DFT software and ATE hardware.

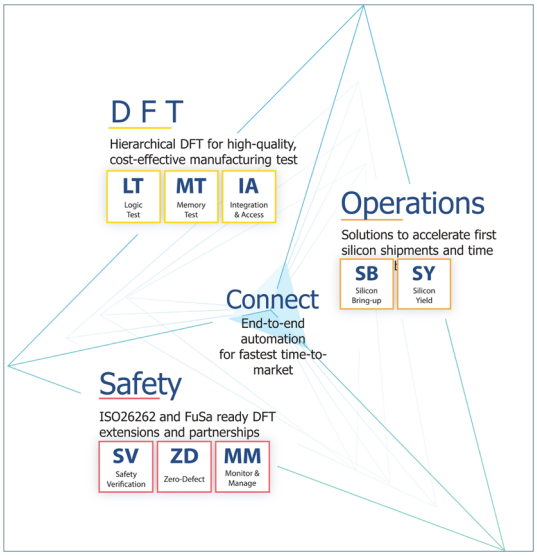
Tessent SiliconInsight can greatly increase productivity during silicon validation and debug, speeding time-to-market.



Tessent siliconInsight.

Tessent silicon lifecycle solutions

Design augmentation and linked applications that detect, mitigate and eliminate risks throughout the IC lifecycle, helping customers address their debug, test, yield, safety, security, and optimization requirements for today's most complex SoCs.



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