SIEMENS
Ingenuity for life

Tessent SiliconInsight

Test bring-up, debug, and characterization

Benefits

- Increase productivity during critical silicon validation and debug phases
- Eliminate costly errors causing increased cycle time
- Enable low-cost, high-availability characterization with the Desktop environment
- Remove barriers to debugging on automated test equipment with ATE-Connect
- Award-winning customer support ensures success

Features

- Interactive control, debug, and characterization of ATPG-tested logic, BIST-tested memories, logic, and IEEE 1687 IJTAG instruments.
- Memory BIST: Determine failing memory, memory port, row and column, address and bit position, algorithm and algorithm phase, and map them to (X,Y) chip coordinates.
- Logic BIST: Determine failing BIST segments, test patterns, and flops. Automatically perform gate-level diagnosis.

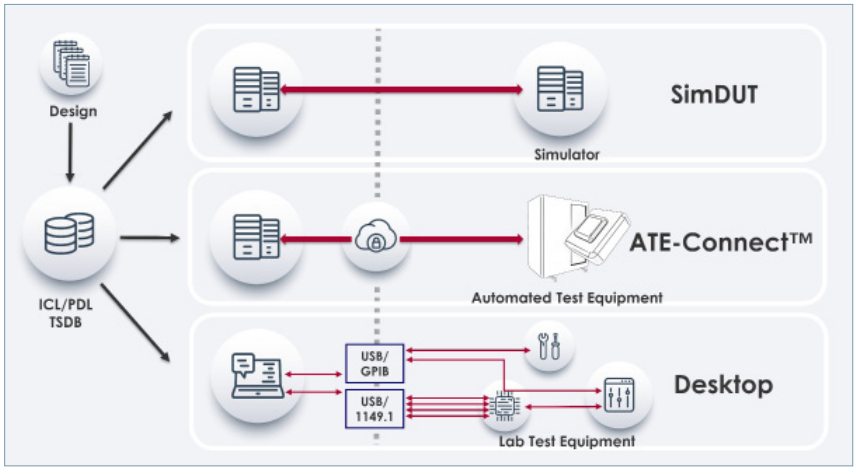
Interactive test debug environment

Silicon bring-up requires significant learning and is prone to errors causing increased cycle time. Reducing the silicon bring-up phase is critical in getting ICs into the hands of customers. Tessent™ SiliconInsight™ in Tessent Shell provides an automated interactive environment for test bring-up, debug, and silicon characterization of devices containing Tessent ATPG, EDT, BIST, and/or IJTAG test structures. Tessent SiliconInsight boosts productivity for chip designers and test engineers during silicon validation and debug, speeding time-to-market.

Diagnosing and interacting with embedded components under test

The interactive environment enables debug and characterization of embedded memories, logic, and IEEE 1687 IJTAG instruments tested using the Tessent TestKompress™, FastScan™, BIST and IJTAG products. Tessent SiliconInsight provides a visual representation of the test resources within the device and the order in which they are to be executed.

Tessent SiliconInsight builds on the Tessent Shell platform, which enables automation and integration of test execution, diagnosis, and pattern generation. The software instantly maps failures to the failing test resource(s), and allows diagnosis down to failing memory cell, scan cell, or net segment.



The Tessent SiliconInsight interactive environments: Test pattern validation before first silicon, debug of IJTAG devices on ATE, and debug using a local desktop environment.

Tessent SiliconInsight

Features *continued*

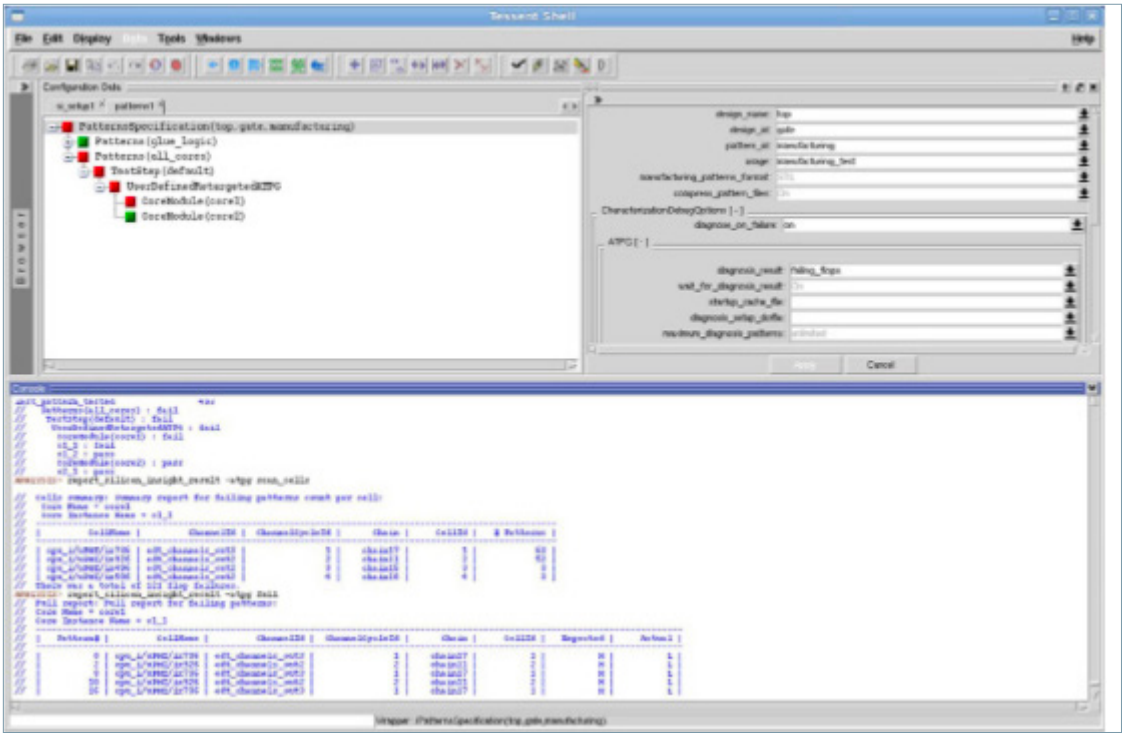
- ATPG / EDT: Determine failing core, scan cells, and failing patterns. Pattern re-targeting and fail file reverse mapping automatic for hierarchical designs. Perform layout- aware and iterative diagnosis.
- Desktop support through access to up to 120 device pins using 3rd party USB adaptors. Shmoo capability of power and clock through GPIB.
- Powerful TCL scripting environment enabling automation, results introspection, and integration with other products on the Tessent platform.
- Interactive IJTAG and MBIST diagnosis on local or remote automated test equipment with ATE-Connect™.

In the desktop use case, Tessent SiliconInsight provides capabilities for performance characterization. The use of GPIB instruments allows measuring of an embedded component's performance across any voltage and/or frequency range. This is very powerful in determining specific design areas that are the slowest and thus limit the overall performance of the design. The solution works in a bench-top environment and connects to any debug, performance, or bring-up board, accessing up to 120 device pins. BIST and IJTAG is accessed through an IEEE 1149.1 compliant TAP controller. Power supplies and clock generators are controlled through the IEEE 488 standard GPIB interface.

ATPG and scan compression

Patterns generated with Tessent can be executed and diagnosed from within Tessent SiliconInsight. Scan pattern retargeting / failure file reverse mapping is fully supported for hierarchical designs.

Diagnosis patterns are automatically generated and executed when required. The following results are available: Failing cores – for hierarchical ATPG, failing scan cells for compressed/ uncompressed ATPG, failing scan patterns, logical suspect / physical defect (requires Tessent Diagnosis). The results are available in Tessent Shell data structures, which makes it possible to create complex characterization experiments and integrate test generation, execution, and analysis.



Tessent SiliconInsight enables interactive debug and characterization.

Logic BIST
Four levels of automated static and at-speed logic diagnosis are provided with logic BIST.

Memory BIST
Get instantaneous analysis of failing memory, memory port, and memory I/O information. When data logging is requested, a detailed report is provided for all failures encountered: The failing memory port, the failing row and column addresses and bit position, the algorithm used to test the memory, and the phase of this algorithm in which the failure was detected. Physical (X,Y) locations can be provided to facilitate failure analysis.

Offline volume diagnosis of MBIST, LBIST
In a production test environment, SiliconInsight generates diagnosis results from volume ATE fail data based on pre-generated diagnosis patterns and an off-line utility that converts failing tester cycles to bitmap information.

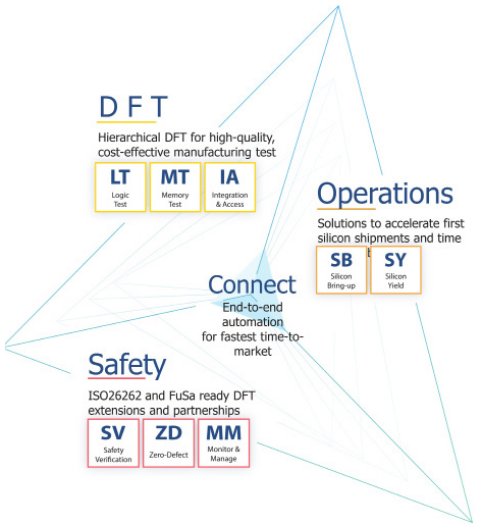
Following a similar off-line flow, LBIST offline diagnosis allows failure data collection on the tester and then interpretation off the tester with SiliconInsight.

SimDUT
Validate test patterns before first silicon. Using the design in a standard simulator, inject faults, characterize potential failure scenarios without silicon.

ATE-connect
Enables direct interaction with IJTAG devices directly on automated test equipment (with validated interface).

- TCP/IP interface for secure communications on customer VPN.
- Send IJTAG PDL Level-0 and Level-1 commands and receive values to debug in real time across the globe.

Tessent silicon lifecycle solutions
Design augmentation and linked applications that detect, mitigate and eliminate risks throughout the IC lifecycle, helping customers address their debug, test, yield, safety, security, and optimization requirements for today's most complex SoCs.



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