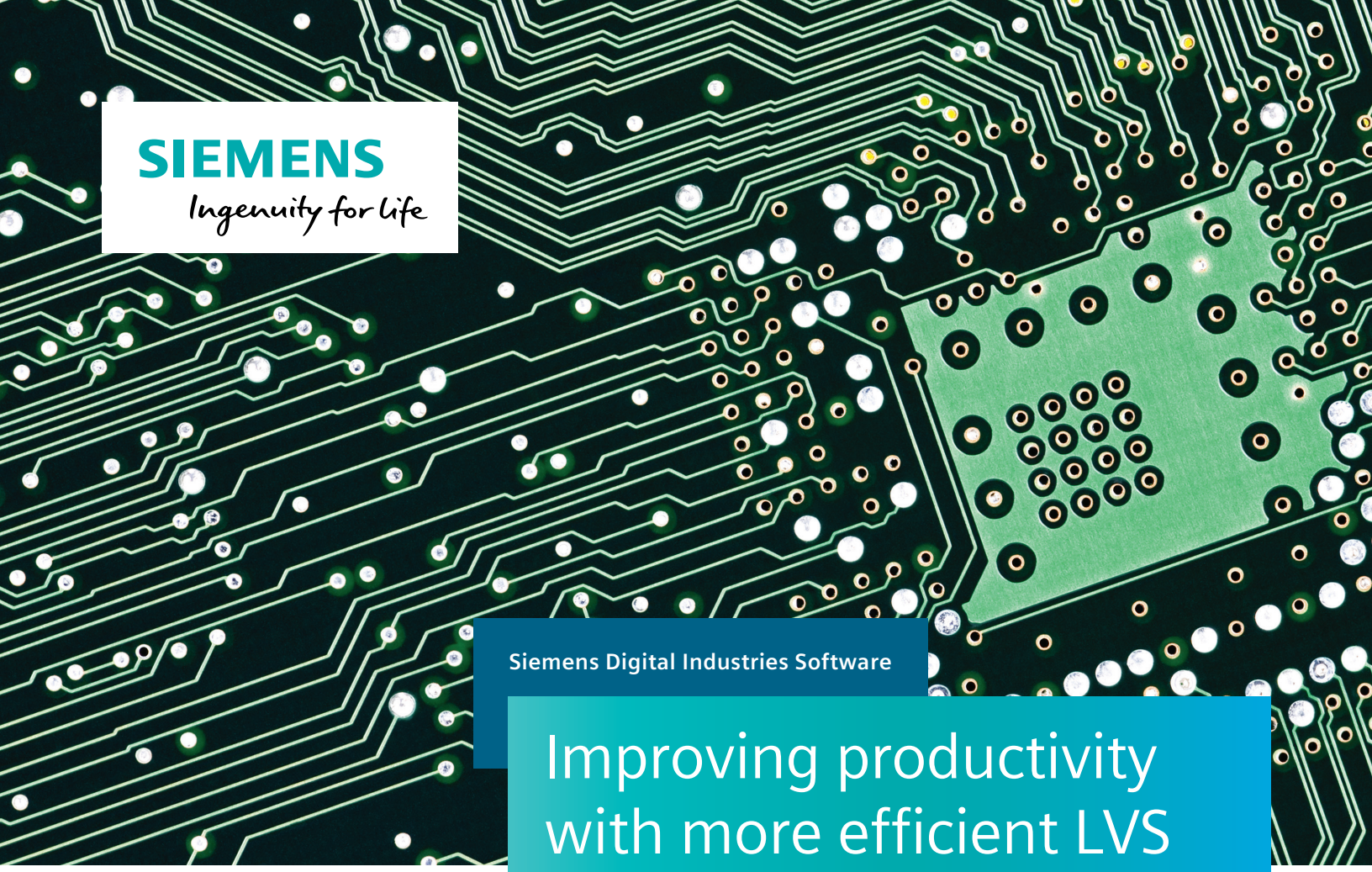


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Improving productivity with more efficient LVS debug

Executive summary

Calibre RVE utilities help designers debug and fix LVS errors more quickly, while also eliminating the need for multiple full LVS runs. Interactive short isolation provides a systematic and prioritized shorts debugging process. Fix suggestions in plain text help designers find the root cause of LVS comparison discrepancies, while the ability to highlight discrepancies in both layout and schematic views lets them implement fixes quickly and efficiently.

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Introduction

Layout versus schematic (LVS) verification is an essential and integral part of integrated circuit (IC) verification in a system-on-chip (SoC) design cycle, but with today's highly dense and hierarchical layouts, increasing circuit complexity, and intricate foundry rules, running LVS can be a time-consuming and resource-intensive endeavor. Full-chip LVS runs not only compare the design layout against the schematic netlist, but also typically include additional verification, such as electrical rule checking (ERC) and short isolation, that increase LVS runtimes.

Debugging LVS results for these designs can be equally challenging and time-consuming depending on the complexity of the design, which can impact the overall turnaround time (TAT) and the planned tapeout schedule. Resolving shorts between power-ground nets can be difficult and time-consuming, due not only to the nature of these large nets with power-ground grids extending across the entire design size, but also because there can be many different causes for a short. Similarly, identifying comparison discrepancies between layout and schematic can be hard, as there can be many causes for the discrepancies, and keeping track of corresponding elements in highly dense designs can be laborious. Implementing an effective and efficient methodology for LVS debug is crucial for designers who want to get LVS-clean results for their high-performance designs in the fastest closure time possible.

Challenges of LVS debug

Traditionally, LVS is a process dominated by two steps: extraction and circuit comparison. First, a layout netlist is extracted from the layout using device extraction and net connectivity extraction. Next, this extracted layout netlist is compared to the schematic netlist. Errors found in either steps can contribute to longer debug time.

Due to the assignment of multiple text names to the same net, texted shorts may occur, leading to the wrong net name being extracted during connectivity extraction. Shorts between texted nets are one of the major debugging issues faced by designers during the extraction phase. Debugging these shorts can be tricky, given that they can have many different causes and can cross design hierarchies. Large nets like power and ground nets can often extend over the entire layout area, containing many polygons and spanning multiple hierarchies, making a shorted power-ground net difficult to debug.

Issues can also arise when comparing the extracted layout netlist to the source netlist. Because today's designs are significantly complex, with numerous devices and multiple hierarchies involved, designers often need significant time to match the equivalent elements in the layout and source netlists, and eventually track and resolve the source of discrepancies.

Whether designers are confronting shorts on a long power net, or debugging comparison mismatches, more effective and efficient debugging techniques are required. Fortunately, designers can take advantage of advanced debug technology to considerably reduce the turnaround time for debugging LVS errors. Let's look at some debug techniques that more efficiently address these complex LVS debugging issues, using the Calibre® toolsuite.

Interactive short isolation

As discussed, debugging shorts in today's designs can be time-consuming, given that shorts can have many different causes and cross design hierarchies.

By initiating a Calibre nmLVS™ run with short isolation enabled, designers can generate a shorts isolation database containing a comprehensive list of all the shorts in their layout. They can then use the Calibre RVE™ interactive short isolation (ISI) debug flow to display the individual polygons extracted for shorted nets, and systematically debug the shorts in a progressive order, starting with the critical shorts first (figure 1).

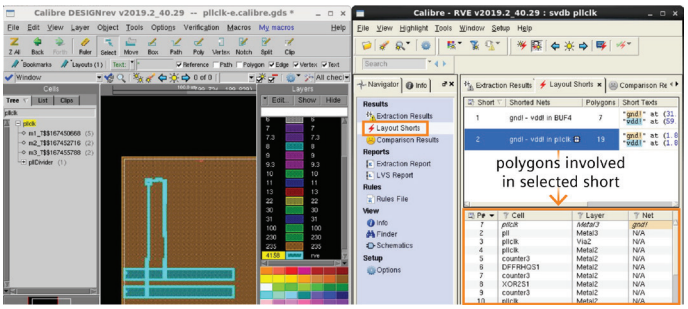


Figure 1: Designer can select and highlight a short, and review the polygons making up the short.

To demonstrate how the Calibre RVE ISI function enables designers to more quickly analyze and correct shorts in a layout, let's walk through the debug of a power-ground short. Designers select the Layout Shorts results list, then select and highlight one of the displayed shorts to view all the polygons involved in a layout editor (such as the Calibre DESIGNrev™ interface). Next, designers assign a net label (vdd! or gnd!) to each polygon, based on their knowledge of the layout and design. Labels can be assigned in the Calibre RVE list, or by labeling the polygon in the Calibre DESIGNrev display. When designers think they have identified the offending polygon, they assign that polygon a REMOVE label (figure 2).

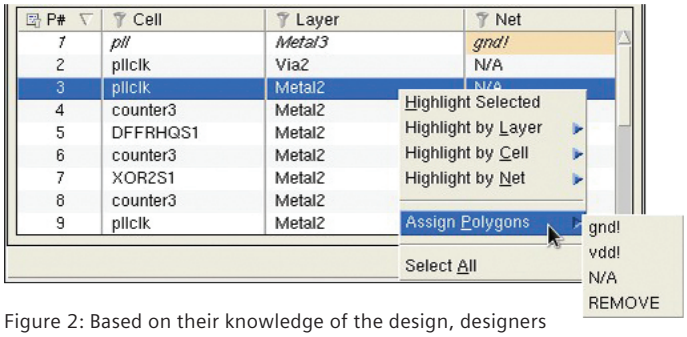


Figure 2: Based on their knowledge of the design, designers assign the appropriate labels to the polygons.

Once all the polygons in a short are labeled, designers can use the ISI Verify Short option to virtually determine if removing the polygon labeled "REMOVE" fixes the short (figure 3). The Verify Short feature uses the extraction information already present in the shorts database to initiate a shorts verification run (not a full LVS run) that determines whether or not the short would be eliminated if the polygon marked REMOVE was not present in the shorts database. This Verify Short process does not actually remove the polygon from the layout; it simply removes the polygon from the shorts database during the verification run.

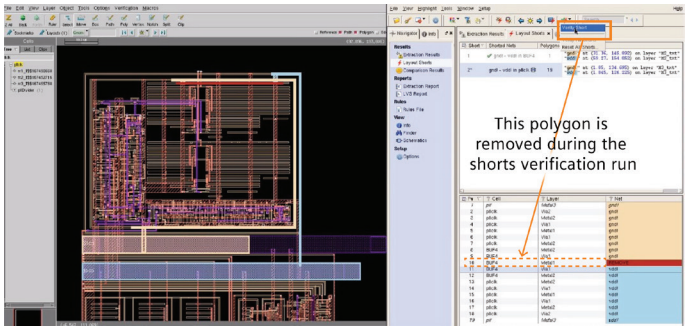


Figure 3: After appropriate assignments, designer can initiate the "verify short" feature.

If the verification run demonstrates that the shorted path no longer exists, and there are no other shorts between the two nets, the short is shown as virtually fixed. If the verification results show that one or more shorts still exist at other locations between the two nets, a new set of the polygons comprising the shorted path are shown. Designers can continue working with this new set of short polygons until they zero in on the offending short polygons. At any stage of the analysis, if they believe they have removed the wrong polygon(s), designers can opt to revert back to the original shorts database and start the analysis over again.

Once all the offending polygons are identified and the short is virtually eliminated, designers must physically remove the shapes from the layout using a layout editor, and initiate a full LVS run to confirm that all the shorts have been corrected. By using the Calibre RVE ISI process, designers can more quickly and systematically debug and fix shorts without the need for multiple full LVS runs.

Comparison discrepancies

After isolating and removing shorts in the extraction phase, designers often encounter discrepancies in the comparison phase. Examples of LVS discrepancies include cross-connection errors, bad instance connection errors, open circuit errors, short circuit errors, and pin swap errors. Debugging comparison discrepancies between the layout and schematic typically requires designers to manually track and manage the corresponding elements while analyzing each discrepancy for its root cause. In highly dense designs, this can quickly become a timeconsuming and frustrating exercise.

To speed up and improve discrepancy debugging, designers can use the Calibre RVE fix suggestions to view the possible source of each discrepancy. These fix suggestions can help designers perform detailed error analysis more quickly by suggesting likely causes for a discrepancy. We'll use a simple pin swap error to show how designers can use these fix suggestions for faster, more efficient discrepancy debugging.

Pin swap errors occur when two layout pins of an instance are cross-connected. Once the layout/schematic comparison is complete, designers can view the Calibre RVE fix suggestion for debug assistance. A clear textual explanation of each discrepancy is presented (figure 4).

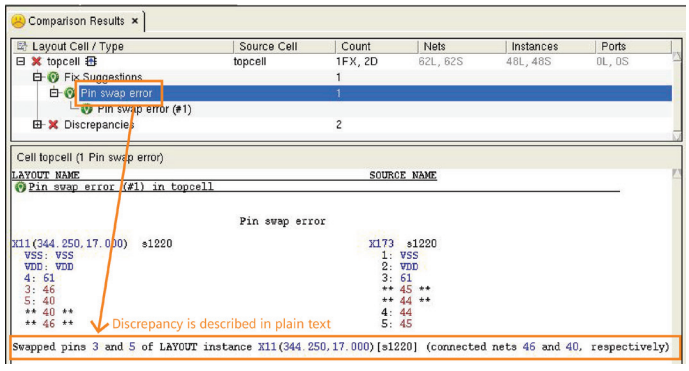


Figure 4: Simple description referring to the possible origin of discrepancy is shown.

In this case, the designer can highlight the instance (X11) and the two nets (46 and 40) involved in the discrepancy in both the layout design environment and the Calibre RVE internal schematic viewers (layout and source). Comparing the internal schematic views enables designers to quickly and visibly see the swapped connections (figure 5).

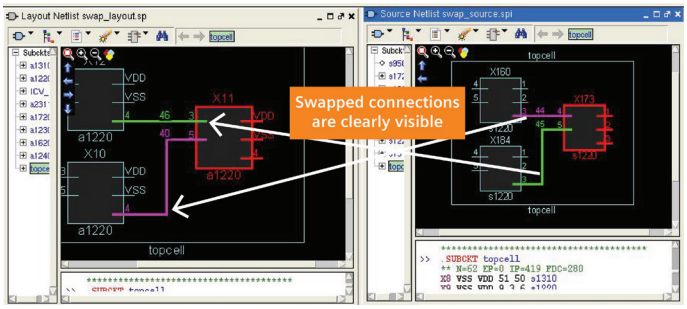


Figure 5: Highlight in internal RVE schematic viewers helps in visualizing the discrepancy.

By referencing the layout highlight with the highlight from the layout schematic viewer, designers can quickly see which connection must be corrected (figure 6).

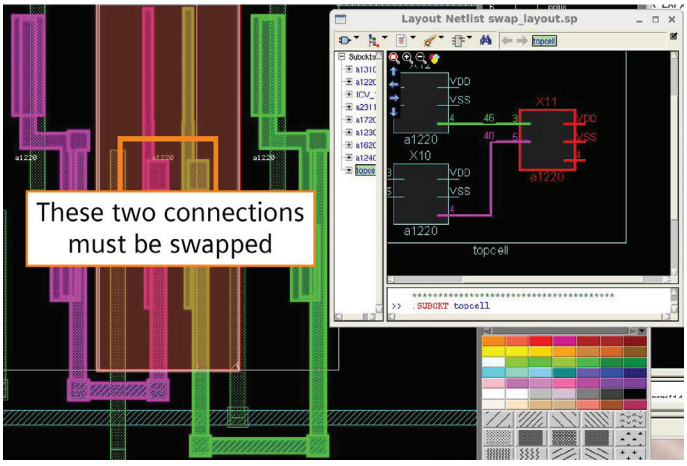


Figure 6: Viewing highlight in layout vs. layout schematic viewer shows which connections must be swapped.

The fix suggestions feature speeds up and simplifies the debug process by providing a clear explanation of the root cause of the discrepancy in simple language. With this information, designers can then use the Calibre RVE layout and schematic viewers to correct the comparison discrepancy faster and more efficiently.

Conclusion

LVS debug is an essential part of the physical verification process. As a signoff requirement, the productivity of LVS debug directly impacts the project plan and tapeout schedule. With today's dense designs and complex rules, the process can be daunting and time-consuming, unless designers take advantage of debugging options and techniques that can make it faster and more efficient.

The Calibre RVE results viewer provides utilities that help designers implement a systematic methodology to narrow down the source of errors and get to their LVS-clean results more quickly. The Calibre RVE ISI capability lets users step through shorts in a controlled and prioritized process to quickly find and remove short sources. In the comparison phase, the fix suggestions feature provides valuable suggestions that help designers debug comparison discrepancies more quickly and efficiently by pointing to the possible source of each LVS discrepancy. Designers can then take advantage of layout and schematic viewer highlighting to locate the origin of each discrepancy and implement corrective action.

By eliminating the need for multiple full LVS runs to verify short fixes, and providing helpful information that enables designers to more quickly identify and resolve the root cause of LVS discrepancies, the Calibre RVE interface enables design teams to complete LVS verification more quickly and confidently, while contributing to an overall reduction in tapeout schedules.

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