Executive summary
Embarking on advanced SoCs without a smart design-for-test (DFT) strategy can be harmful to your bottom line. Being competitive in today’s semiconductor market means adopting integrated, scalable, and flexible solutions to cut DFT implementation time, test costs, and time-to-market. Tessent™ DFT technologies, developed in partnership with industry leaders, provide the most advanced DFT and yield solutions available. This paper describes the most significant areas of Tessent DFT research and development that enable semiconductor companies to produce competitive products. We include examples of how Tessent solutions are being applied to some of today’s most challenging designs, like extremely large artificial intelligence (AI) processors and ICs for automotive applications.

Ron Press, Siemens EDA
Introduction

The semiconductor industry has been able to deliver dramatic advances in IC capabilities by refining and optimizing all aspects of design and fabrication. Design-for-test (DFT), which includes everything from the insertion of test logic in the RTL to failure analysis of field returns, is a vital part of a semiconductor business success. Without an effective DFT strategy companies struggle to keep up with the huge demands on DFT integration, defect detection, and fabrication process/yield improvements.

Any of these demands can interfere with a product’s viability in the marketplace. For some products, DFT is now part of the functional system requirements. To stay competitive in the semiconductor industry, companies need to partner with a DFT solution provider that is low risk, trustworthy, and has a proven track record of co-developing scalable technologies with their partners that work in a variety of design flows.

Focusing on these types of challenges with our partners has made Tessent the clear market leader and a “safe choice” DFT solution provider. Our strong partnerships across the semiconductor ecosystem also make Siemens Digital Industries Software well positioned to continue advancing DFT technology for future needs.

Today, companies need to employ a few fundamental DFT capabilities to remain competitive. The basic DFT needs include:

• Employing the most effective techniques for detecting manufacturing defects.
• Implementing solutions that efficiently integrate into various common design flows and functional system requirements.
• Leveraging DFT and production test results to improve yield which directly impacts both time-to-volume and profitability.
Most recently, DFT is playing a key role in the creation of Silicon Lifecycle Solutions (SLS). The core concept behind SLS is to create an infrastructure that gathers data throughout the design, realization and deployment of a product; and to provide feedback and feedforward loops to allow that data to be used to augment all aspects of the product's performance. For details, see Tessent Silicon Lifecycle Solutions: Enabling the next step in IC test and monitoring.

The benefits of SLS are wide ranging – from improved manufacturing efficiency to better device cybersecurity; from reduced in-field maintenance costs to the creation of new “fleet-based” models of product and service delivery.

To enable the SLS approach, Siemens has added functional monitoring and analytics capabilities to the Tessent product family, in the shape of its Embedded Analytics technology. Embedded Analytics provides a scalable functional monitoring platform that includes a portfolio of silicon IP together with software interfaces, APIs, an SDK, and database and IDE functionality.

Embedded analytics enable real-time monitoring and analysis of the functional behavior of complex ICs at any level of detail – from the complete SoC to individual instructions and bus transactions, and with a unified view of hardware and software operation. For more information, see Embedded Analytics: A platform approach.

Good engineers base decisions on hard data. This paper describes the most significant areas of DFT research and development that enable semiconductor companies to produce competitive products. We show how those solutions are being applied to some of today’s most challenging designs, like extremely large artificial intelligence (AI) processors that require hierarchical plug-and-play methodologies, and automotive applications that need very high manufacturing test quality and in-system test capabilities.
Detecting defects

The core function of DFT is to catch defects in manufactured silicon and ensure that a part will operate as designed once it’s placed in-system. Defect coverage is the percentage of all possible defects that a manufacturing test can detect and can be expressed in a well-known formula (Williams, 1981) to predict the defect level depending on the process yield:

\[
\text{Defect Level} = 1 - \text{Yield}^{(1-\text{Defect Coverage})}
\]

The defect level is most commonly expressed in terms of defective parts per million (DPPM). If you fail to detect defective products and ship too many bad parts, then your entire business can suffer.

Table 1 shows how different manufacturing process yields dramatically affect the DPPM rate even if 99% defect coverage is achieved. Achieving 99% defect coverage might sound pretty good. From Table 1, though, you can see that even for a mature process with a 90% yield, a 99% defect coverage results in over 1000 DPPM. For many of today’s automotive and functional safety products, that is an unacceptably high DPPM rate. At the same 90% process yield, you would need to reach 99.9% defect coverage to get to 100 DPPM and 99.99% defect coverage for 10 DPPM.

Table 1 – Process yields dramatically affect the DPPM rates.

<table>
<thead>
<tr>
<th>Process yield</th>
<th>Defect coverage</th>
<th>Defect level DPPM</th>
<th>Defective PPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>0.99</td>
<td>0.00105305</td>
<td>1053</td>
</tr>
<tr>
<td>0.8</td>
<td>0.99</td>
<td>0.002228948</td>
<td>2229</td>
</tr>
<tr>
<td>0.7</td>
<td>0.99</td>
<td>0.003560396</td>
<td>3560</td>
</tr>
<tr>
<td>0.6</td>
<td>0.99</td>
<td>0.005095231</td>
<td>5095</td>
</tr>
</tbody>
</table>

Table 2 shows how different defect coverage levels affect DPPM when the process yield is 80%.

Table 2 – Defect coverages and DPPM at 80% yield.

<table>
<thead>
<tr>
<th>Process yield</th>
<th>Defect coverage</th>
<th>Defect level DPPM</th>
<th>Defective PPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.98</td>
<td>0.004452927</td>
<td>4453</td>
</tr>
<tr>
<td>0.8</td>
<td>0.97</td>
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<td>6672</td>
</tr>
<tr>
<td>0.8</td>
<td>0.96</td>
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<td>8886</td>
</tr>
<tr>
<td>0.8</td>
<td>0.95</td>
<td>0.011095167</td>
<td>11095</td>
</tr>
</tbody>
</table>

The Williams formula makes it look simple to predict DPPM rates, but it can be difficult to apply this equation because the variables are hard to know precisely. Defect coverage refers to the entire universe of potential defect types, including known fault models such as stuck-at, transition delay, path delay, IDDQ, bridging, cell-aware, and more. The cell-aware fault model has been developed for over 15 years to effectively perform defect-based fault modeling to detect potential defects within technology cells. There have been many publications from industry leaders on the value of this technology to real products, with a dramatic impact on DPPM, including AMD (Hapke, 2014).

Advances have been made in defect-oriented test, which are fault models based on the physical design that identify where defects can occur. It is also referred to as “automotive-grade” ATPG. These developments enhance cell-aware test and provide new types of bridge, opens, cell-aware/timing-aware (figure 1), and cell-neighborhood tests. Silicon results were published showing the significant value of cell-aware test and automotive-grade ATPG by Intel (Howell, 2018) and ON Semiconductor (Maxwell, 2017). You can watch the recorded ITC session on Intel’s experience with defect-oriented test.

These new pattern types are not just for special cases or automotive-level DPPM requirements. However, with unique silicon detection results in the 1000+ DPPM ranges, many companies have standardized on cell-aware tests and no longer apply stuck or transition patterns.
Memory built-in self-test (BIST) is used to detect failures within embedded memories and their interface logic. The biggest challenges for memory BIST are not new technologies or new types of memories, but the industry trend for more on-chip storage capabilities, which now reaches well beyond the Gbit range of embedded SRAM spread across well over 10,000 memory instances.

Managing memory BIST DFT for designs with a very large number of memory instances is best achieved with a hierarchical DFT methodology. Hierarchical DFT for designs of this scale requires fully automated solutions that can take general user directives across all parameters (test time, area consumption, power consumption, etc.). Further, (shift) access time to each memory BIST controller and, in particular, access to fail data for volume diagnosis of memory test failures becomes a considerable component of memory BIST DFT planning.

Tessent works very closely with IC designers and memory providers to continuously validate our memory BIST solution on the latest technologies and memory designs. As a result, our standard library algorithms continue to provide the highest level of defect detection. A significant amount of flexibility is built into the memory BIST capabilities to enable custom algorithms for various styles of memory design. With nearly every design containing repairable memories, Built-In Repair-Analysis (BIRA) and Built-In Self-Repair (BISR) are commonly used, even in-system.

Enabling technology

Achieving acceptable defect rates requires targeting various types of defects using different fault models, but it comes with a practical cost. Take, for example, the effect of the 130 nm process, developed in 2001-2002, on DFT. It introduced a new process and new materials (copper) that resulted in defects that were only seen when operating at-speed. Up to that time, high coverage for stuck-at faults was considered a sufficient test. With these new at-speed defects, though, it suddenly became necessary to perform at-speed tests using the transition delay fault model and sometimes path delay as well. As a result, the test pattern count exploded, leading to significant test costs as more manufacturing test equipment was needed to keep pace with the demand.
It was at this time that Tessent TestKompress first introduced embedded compression technology (Rajski, 2004) allowing more patterns to be tested with less tester memory. Improvements to TestKompress compression levels remain a constant focus of development because Moore’s Law continues to drive design sizes high and new technologies result in new defect types requiring more patterns. Special test points were introduced that dramatically reduced pattern sizes often by 5x as published by Broadcom (Konuk, 2015) to help control the growing pattern counts. The inclusion of LBIST for in-system test and MBIST for high-quality memory testing are essential for the designs requiring them.

Another advancement in recent years provides a method to figure out which patterns are most effective between various pattern sets targeting different fault models. Now critical area can be used to consider the likelihood of defects occurring to assess the value of patterns between different fault models for an apples to apples comparison. In addition, multiple fault models can be targeted within one ATPG run resulting in up to 40% smaller pattern set. For details, see the paper Critical area based test pattern optimization for high-quality test.

Leveraging DFT to Improve Yield

Reducing the number of failing die and improving the reliability of the manufacturing process has a direct impact on business. But getting there isn’t simple. Challenges like growing design sizes, shrinking time to market, and new defect types and behaviors with new technology nodes.

Structural test patterns are used to detect failing die before they are shipped to customers, and the data from the failing tests provides valuable information about the mechanism(s) causing the die to fail that can be leveraged to improve yield faster. A thorough analysis of failing scan test data—called scan diagnosis—is regularly used by companies that own their fabrication facilities, pure-play foundries, and fabless semiconductor companies.

Scan diagnosis produces a set of defect suspects and highly localized defect locations that explain the failing scan tests for that die. This detailed information improves the success of the physical failure analysis (PFA) used to validate the defect mechanisms. Tessent Diagnosis has been used successfully to guide the PFA process to find a root cause mechanism. GLOBALFOUNDRIES reported over 10x better resolution with this approach (Benware, 2012).

Analyzing and fixing a yield problem implies understanding the failure/defect mechanisms not only on individual die but also the failure mechanisms across an entire population of dies. These populations (of failing die) can span several wafers or even lots. Using scan diagnosis for insight into yield limiters confers a competitive advantage that can impact profitability.

In newer technology nodes, the defects in the front end of line (FEOL) are commonly the dominant part of the defect distribution.

Companies implementing new fabrication processes have to quickly determine yield limiters, especially if they are related to a specific cell layout or geometry. Leveraging the data created for cell-aware test, Tessent Diagnosis can point to defect locations and types inside of standard cells. The defect pareto generated by Tessent YieldInsight can have either FEOL or back end of line (BEOL) root causes when cell-aware diagnosis is in use (Tang, 2019).

Reducing the yield excursion cycles can also affect profitability. Fabless customers who own the design can continually generate volume diagnosis results, analyze those results, and correlate those with PFA findings. These volume scan diagnosis results can be used to track defect paretos over time. Foundries can also leverage the results of the defect pareto from volume scan diagnosis to correlate with other data sources to understand the source of an excursion. This collaborative approach can lead to a quicker turn-around time in solving excursions.
DFT Methodology Advances
With the growth in design sizes, design flows have become more hierarchical, creating design cores that are functionally complete all the way through physical design. The finished blocks are then instantiated into the top level of a chip, or to chiplets then to chip top. Companies that tried to continue with full, flat ATPG or partitioned-based approaches with manual steps suffered severe time-to-market delays. Breaking designs into smaller pieces makes physical implementation more manageable for designers as well as for automation tools.

Hierarchical DFT also lets you take advantage of cores that have many identical instantiations, as seen in many AI designs. All the design effort goes into one instance, which can then be instantiated as many times as required. DFT also benefits from a similar divide-and-conquer approach that is consistent with the rest of the design flow and addresses the same problems with large designs.

Tessent Hierarchical DFT was introduced so that not only can physical design blocks be functionally complete, but DFT complete as well. This methodology requires a few key technologies such as core wrapping for core isolation, graybox model generation to reduce machine memory consumption, and pattern retargeting to re-use core level generated patterns.

The move to hierarchical DFT has demonstrated dramatic improvements in all aspects of DFT. Amazon explained how hierarchical DFT took their DFT work out of the design critical path to tapeout (Trock, 2016). Samsung summarized the improvements in run time, pattern count, and compute resources in figure 2 (Shin, 2019). They saw an order of magnitude improvement by adopting this hierarchical DFT methodology. For large SoC designs, hierarchical DFT has become the standard practice.

Tessent Streaming Scan Network (SSN) takes plug-and-play DFT to the next level. It provides a packetized data delivery bus on top of TestKompress to make core TestKompress optimization completely independent from the core embedding and SSN bus width. It also has completely scalable handling of identical cores utilizing on-chip compare. Significant time to market and test application time results were described by Intel at the 2020 International Test Conference.

For details about the Tessent Streaming Scan Network, see the Siemens paper Streaming Scan Network: A No-Compromise Approach to DFT.

Figure 2: Benefits of hierarchical DFT as experienced on a GPU design (B. Shin, ETS 2019).
Unified DFT Environment

Design practices evolve constantly, and one growing trend is to push as much of the design into the RTL stage because physical synthesis tools produce better timing closure results when they can see all of the design. DFT has historically been considered more of a back-end task but it has been necessary to add more DFT logic like Tessent TestKompress into the design to address test challenges.

As DFT necessarily migrates further upstream into the RTL stage, it becomes increasingly important to merge with the front-end design flow, manage these tasks in a repeatable flow, and maintain design awareness to facilitate downstream integration.

While designs increase in number of cores, DFT functions, and complexity, the designer’s pain and suffering is evident as they try to integrate everything in a simple, low risk, and repeatable manner. EDA tool users might assume that DFT products are all built separately and have to integrate outside of the individual products. This was the case but is no longer true.

With the goal of helping to manage huge and complex designs, Tessent built a platform designed as one tool to control them all. Tessent Connect is the result of almost a decade of development to provide an integrated Tessent platform. It is one tool that can perform all DFT operations such that each DFT function can share the same database and be aware of other DFT functions (figure 3).

As a result, Tessent Connect operates as an “intent-driven” environment, reducing many steps and accelerating time-to-market. Users can work at a higher level of abstraction. The challenge of inserting DFT, creating patterns, and integrating the DFT functions at the top level are all managed in a plug-and-play environment. Without such an integrated platform, companies struggle to manage DFT functions such as BIST during ATPG and would have many steps to integrate core-level DFT and patterns at the top level.

eSilicon discussed the value of Tessent Connect to them when implementing DFT on sophisticated next-generation ASICs (Mentor, 2019). Broadcom, with the goal of fast time-to-market for advanced designs such as AI devices, experienced a 50% reduction in implementation time with hierarchical DFT and Tessent Connect (Mentor, 2020). They described this significant advantage at the 2019 International Test Conference in Washington, D.C.

Figure 3: Tessent Connect provides the type of platform necessary with current levels of complexity and integration.
Value of Advanced DFT for the Semiconductor Industry

Certain technology areas continually push the boundaries of what tools and techniques can do. Today, AI processor designs are typically very large, consist of many duplicate processor arrays numbering in the hundreds or thousands and require high test coverage. There's no way to manage this without a hierarchical DFT methodology that divides the task into smaller pieces. The coverage requirements include many fault models, which means embedded compression must also be aggressive. Graphcore reported being able to have logic BIST, ATPG, and memory BIST up and running in under three days on a 23.6 billion transistor AI chip using hierarchical DFT (Mentor and Graphcore, 2019).

Automotive designs are the most demanding in terms of quality because of the functional safety applications and ISO 26262 standard that must be met. It is vital for companies designing automotive products to have a robust in-system test capability. Tests need to be managed for all built-in self-test (BIST) functions and complete tests very quickly. Arm partnered with Tessent to provide a safety ecosystem (Bush, 2019), which is built on top of the Tessent MissionMode controller and new LBIST Observation Scan Technology, which reduces logic BIST test time by 5x (Tyszer, 2019).

DFT capabilities and implementation are not just dependent on the DFT tools but the ecosystem around them. Tessent has worked closely with partners to develop fundamental and scalable technologies, and Tessent products work in any design flow. We also understand the importance of enabling customers with a solid ecosystem. As a result, Tessent works closely with partners to provide the following ecosystem:

- Arm cell-aware library models for cell-aware test and cell-aware diagnosis (Gahdhi, 2019)
- Arm/Tessent hierarchical reference flow for subsystems containing Arm cores (Press, 2019)
- Samsung foundry SAFE automotive and hierarchical reference flows
- Teradyne and Advantest ATE-Connect over-the-cloud tester access
- Teradyne and Advantest 1149.10 high-speed IO (HSIO) scan test
- Many other reference flows are available from Tessent; many with open-source testcases
Summary

Tessent solutions are carefully developed in close partnership with industry leaders to provide scalable technologies. In particular, providing the ability to create Automotive-grade ATPG and a true hierarchical plug-and-play DFT platform were vital solutions for many companies. The DFT methodologies of old are not effective with the huge designs that exist today. The Tessent platform was developed to integrate all the DFT functions under one tool and one database and with a universal plug-and-play infrastructure for integrating blocks and DFT functions.

Being the market leader and having more resources than all other EDA DFT vendors combined enables Tessent to build future-looking capabilities with partners. The Tessent group works with the majority of leaders in all areas related to semiconductor design and production.
References


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